MODELING OF HIGHER ORDER EFFECTS IN SMALL GEOMETRY MOSFETS

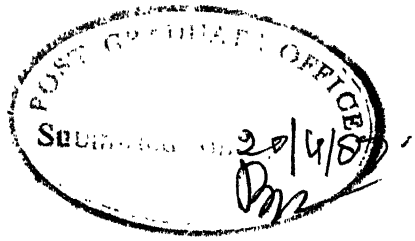
A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

by
DEVESH K. DATTA

to the
DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

APRIL, 1987

EE-1987-M-DAT-MOD



CERTIFICATE

Certified that the work embodied in this thesis entitled, 'Modeling of Higher Order Effects in Small Geometry MOSFETs', is a report of the work carried out by Devesh Kumar Datta, under my supervision and the same has not been submitted elsewhere for a degree.

(M.M. Hasan) 20/4/87
Professor
Department of Electrical Engineering
Indian Institute of Technology
Kanpur

ACKNOWLEDGEMENT

I am extremely grateful and highly indebted to my thesis supervisor Dr. M.M. Hasan, for his guidance and help throughout this work. Accomplishment of the present thesis would not have been possible without his sustained encouragement and open hearted cooperation.

I also take this opportunity to thank my friends for having made my stay so memorable. A special mention of - A.S. Mandal, S. Goswami, N.H. Jafri , M. Kumar and D. Pratihar.

Finally thanks are due to Mr. J.S. Rawat for his excellent typing.

- Devesh Kumar Datta

ABSTRACT

Device modeling has become an indispensable tool in the design and development of complex LSI/VLSI circuits. The main object is to link the physical device parameters to the output terminal characteristics. An accurate model is used to predict the device behaviour without having to go into actual fabrication process. The overall result is the considerable simplification in device design procedures and in the simulation of output performance.

The packing density and performance level consideratio haveled to the design of MOSFETs with very small dimensions. Such small geometry MOSFETs are used extensively in LSI/VLSI digital systems. These small geometry MOSFETs give rise to certain effects which complicate device operation and degrade device performance. It therefore becomes necessary and essential to understand the physical behaviour of such MOSFET and to develop suitable models.

The modeling of higher order effects in small geometry MOSFETs, have been, thus carried out with above mentioned aspects in view. The models developed to account the various higher order effects are based on semiempirical and analytical approach. The reason is to provide a better insight into physical mechanism and also to develop faster computer programs suitable for CAD.

CONTENTS

CHAPTER 1

INTRODUCTION

In the past several years MOS technology has become indispensable in the design and development of large scale integrated circuits and system. Using the MOS devices as building blocks, a vast array of complex integrated system has been designed. Because of its potential for high density, high performance and low power applications, MOS technology has been the tool for the rapid growth and advancement of MOS VLSI systems.

In an effort to increase the silicon real estate utilization the integration density has been increased steadily and when compared to the medium scale integration of a decade ago dramatically, significant part of this steady increase lies in the reduction of the size of the individual devices, and this reduction has been supported by several technological developments such as more accurate process control and fine pattern lithography by optical, electron beam, and ion beam techniques. However as the channel length is reduced, many effects, which, heretofore were of second order importance, became of primary importance and dominate device and circuit performance. The reduction

of the device size in order to achieve greater performance has followed a scaling principle [1], but this approach is limited by physical and practical problems. An insight into some of these problems can often be obtained through the study of models of the device itself.

The technological difficulties involved and the possible innovative solutions have been discussed by a number of authors [2] - [4]. For the present case, main emphasis here is on the study and analysis of various small geometry MOS effects necessary to predict accurately overall device behaviour. One of the basic limitations of size reduction in VLSI is the spacing of the source and drain diffusions i.e. the channel length. Drain potential reverse biases the drain-substrate p-n junction and creates a field pattern that can lower the brarrier, separating it from the source. As the barrier is lowered, additional subthreshold current can flow, and the source-substrate-drain structure acts qualitatively as a bipolar transistor. For a given channel doping concentration, as the channel length is reduced, the depletion layer width of the source and the drain junctions become comparable to the channel length. The potential distribution in the channel now depends on both the transverse field E_x (controlled by gate and substrate

voltage) and longitudinal field E_y (controlled by drain bias). This two dimensional potential distribution is in contrast with original gradual channel approximation ($E_x >> E_y$) for long channel devices. This two dimensional potential results in degradation of various device parameters. The present work emphasizes study of such higher order effects and to provide simple models based on reasonable assumptions.

The study of higher order effects as such is important for the development of CAD models for the MOSFET which would greatly help in more accurate prediction of the device and circuit performance. They would also aid in the simulation of scaled down MOSFETs. Besides it would also be possible to study the influence of specific device parameters on the output behaviour of the basic logic gates. Such studies would significantly contribute towards optimum selection and design of the various device parameters. Finally since actual process dependent effects have been included in the models developed, some indirect link between the electrical behaviour and the fabrication process would also be obtained.

In Chapter 2, a brief discussion on long channel MOSFET theory has been presented. The theory aims to provide

a link between the existing long channel expressions with corresponding short channel relationships described in later chapters. A short introduction to general MOSFET fabrication process is given. This is required to appreciate the various process dependent effects.

Chapter 3 covers the discussion on threshold voltage of small dimension MOSFETs. This includes the models of threshold voltage for short channel and narrow width devices. Also modification due to nonuniformly doped substrate structure has been included.

In Chapter 4, the various small dimension effects have been described, which tends to limit the useful operating voltage range of small geometry MOSFETs.

Chapter 5 covers the conduction behaviour of small geometry MOSFETs at below and above threshold voltages.

In Chapter 6, the influence of threshold voltage variation due to scaling and influence of subthreshold current on circuit performance is discussed.

Finally Chapter 7 presents the concluding remarks and discussions on several relevent aspects. Scope for future work has also been indicated.

CHAPTER 2

MOSFET THEORY

2.1 INTRODUCTION

The schematic diagram of a typical n channel MOSFET is shown in Fig. 2.1, the coordinate system has also been shown, the direction normal to GATE has been taken as x axis whereas y axis is taken along the channel in the direction of current flow, the same convention has been used throughout the present work.

Two n-type regions are diffused into the p type substrate these regions form the drain and source contacts. The gate structure is essentially combined with the p type substrate to form a MOS structure. For a enhancement mode device, with no voltage applied to the gate, the source to drain electrodes correspond to two p-n junctions connected back to back. The only current that can flow from source to drain in this case is, the leakage or subthreshold current. If the gate is biased positively, a negative surface space charge appears at the semiconductor surface next to the oxide. For a sufficiently large forward bias, a n type

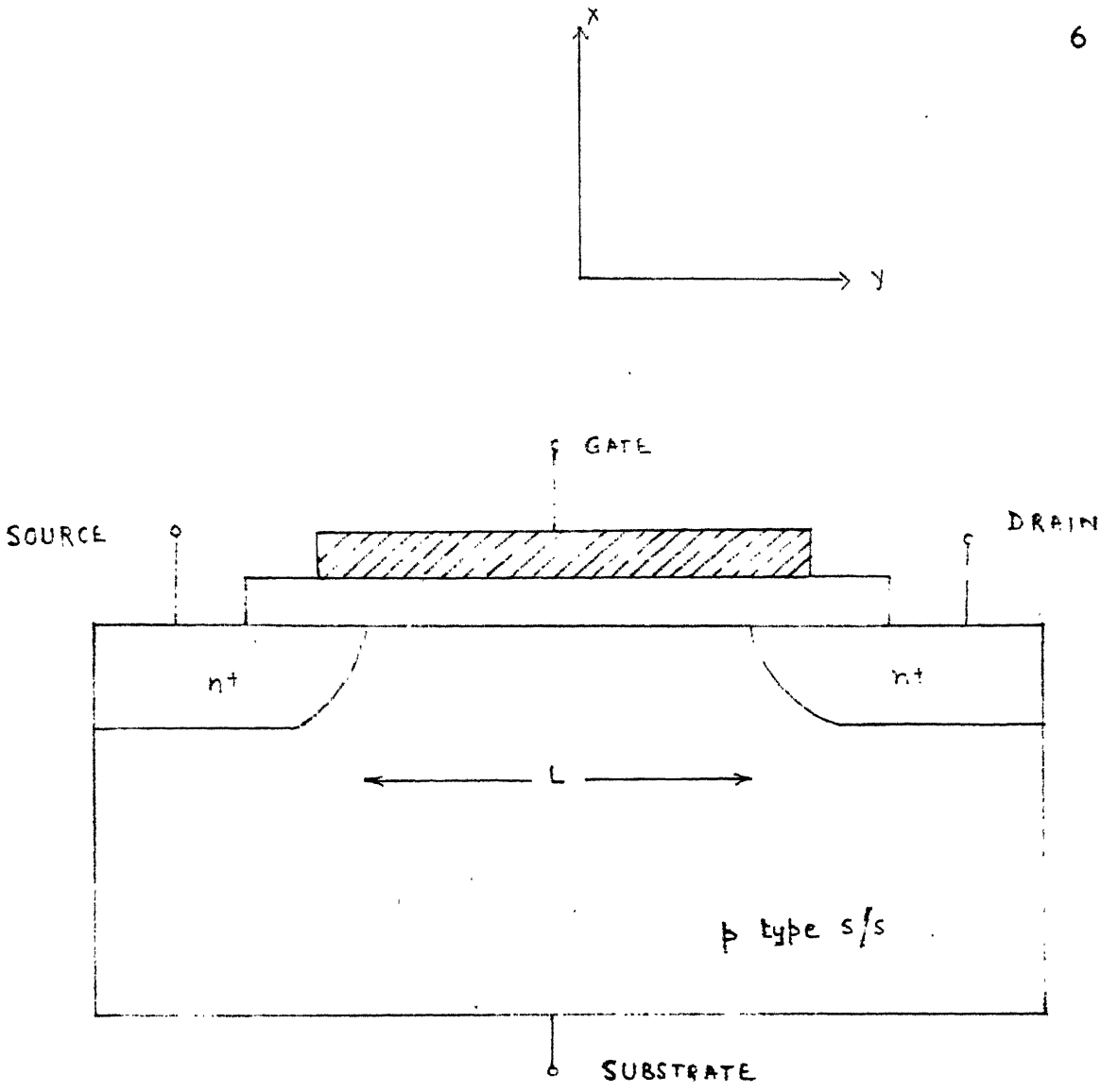


Fig. 2.1 MOSFET Schematic Diagram

inversion layer forms at the surface. This inversion layer forms a narrow channel between the source and drain contacts, and this inversion channel conducts current from the source to drain. The MOS structure modulates this current by varying the surface charge. The depth of the channel into the p-region is determined by the gate voltage and the drain voltage, since it is the difference between voltage accross the region $V_G - V(y)$, where $V(y)$ is the surface potential at y, which determines the surface charge density at that point. The backgate bias or substrate bias also affects the channel conductance.

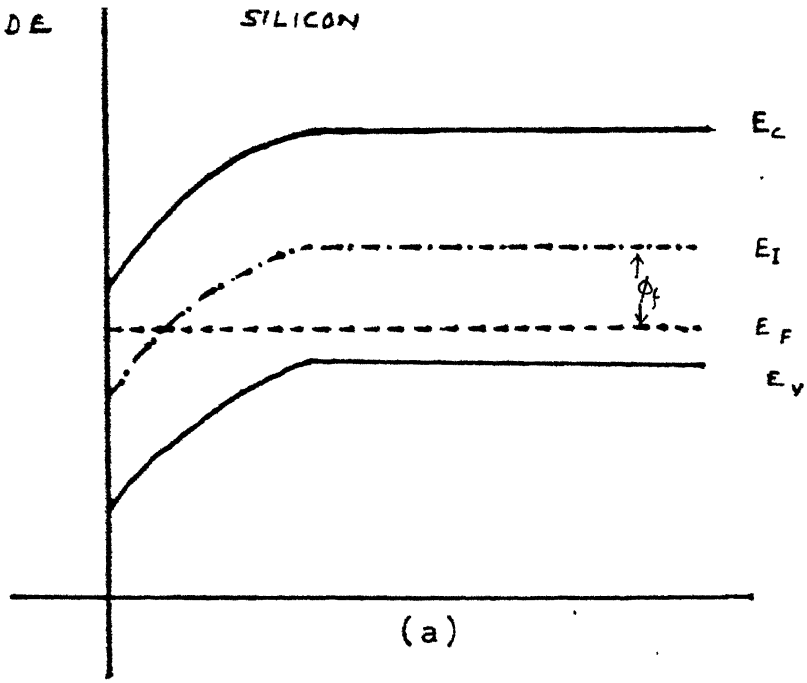
2.2 THE SURFACE POTENTIAL

Formation of the channel at the surface will occur at strong inversion that is when the minority carriers at the surface become equal to the majority carrier density at the bulk $n_s = N_A$ this occurs when

$$\varphi_{s_{inv}} = 2\phi_f$$

with $\phi_f = \frac{kT}{q} \ln \left(\frac{N_A}{n_i}\right)$.

For grounded source and drain voltage $V_{DS} > 0$, surfac



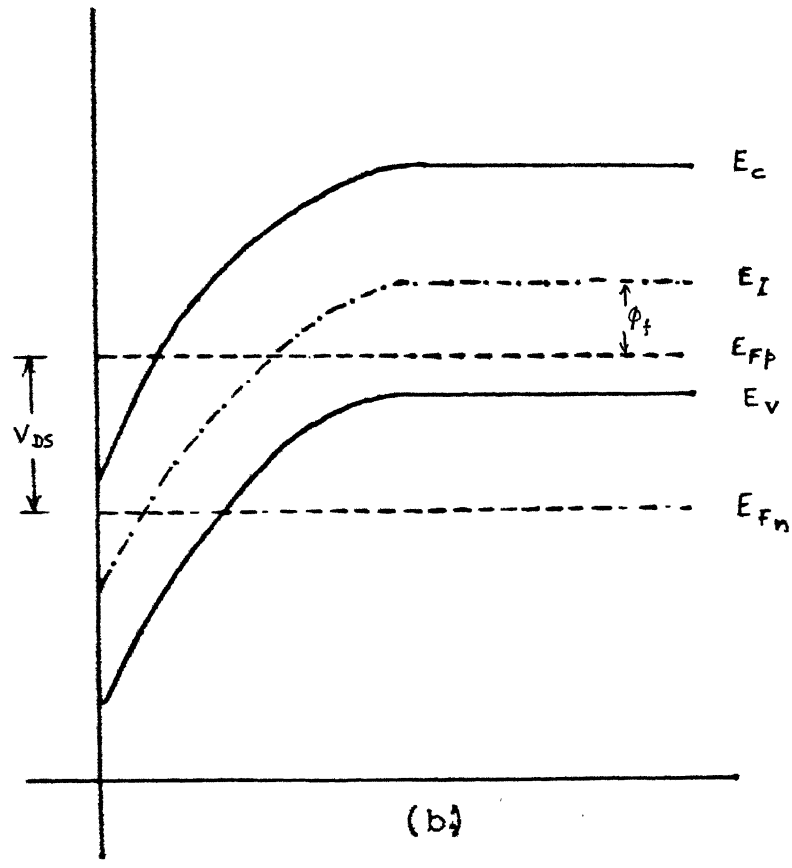


Fig 2.2: Energy Band Diagram of P Type Substrate

(a) At $y = 0$ (b) At $y = L$

potential vary from source to drain, corresponding energy band diagram is shown in Fig. 2.2, obviously

$$\varphi_{s_{inv}}\Big|_{y=0} = 2\phi_f$$

$$\text{and } \varphi_{s_{inv}}\Big|_{y=L} = 2\phi_f + V_{DS}$$

From this it is apparent that the surface potential increases from source to drain, and voltage across oxide layer and channel is a decreasing function of y, as y increases from source to drain. The channel depth decreases along same direction with pinch off occurres at the drain end of the channel.

2.3 THE THRESHOLD VOLTAGE

The voltage applied across the gate appears partly across the oxide and partly across the semiconductor. Thus

$$\begin{aligned} V_{GS} &= \phi_{MS} + V_{ox} + \varphi_s \\ &= \phi_{MS} + \varphi_s - \frac{(Q_{is}+Q_F+Q_B)}{C_{ox}} \\ &= (\phi_{MS} - \frac{Q_{is}}{C_{ox}} - \frac{Q_F}{C_{ox}}) + \varphi_s - \frac{Q_B}{C_{ox}} \end{aligned} \qquad (2.1)$$

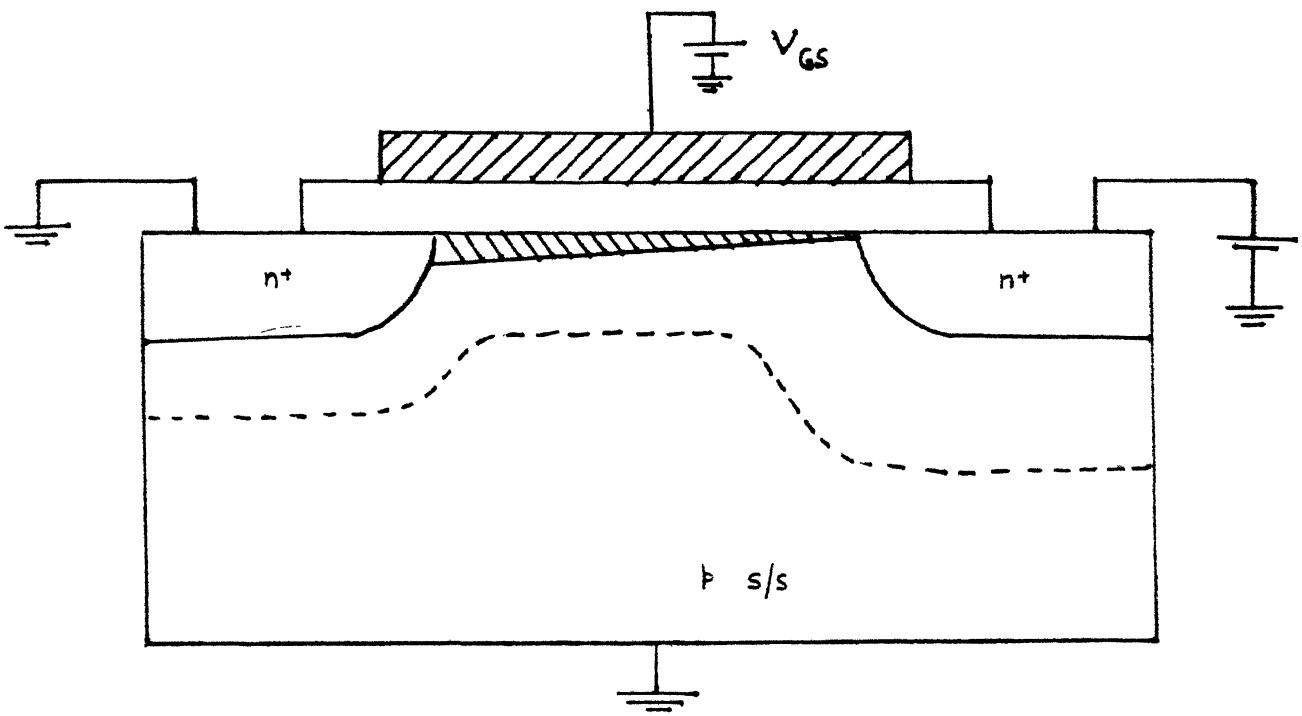


Fig. 2.3 Formation of Depletion Layer and Channl

where,

ϕ_{MS} = metal semiconductor work function difference

Q_F = Fixed oxide charges density

Q_{is} = Interface state charge density

Q_B = depletion layer charge density

C_{ox} = Oxide capacitance per unit area

Threshold voltage, defined as gate voltage at onset of inversion with $\varphi_s = 2\phi_f$

$$V_{th} = V_{FB} + 2\phi_f - \frac{Q_B}{C_{ox}} \qquad (2.2)$$

where V_{FB} = flat band voltage.

2.4 CURRENT VOLTAGE CHARACTERISTICS

Assuming an NMOS device, voltages V_{GS}, V_{DS} and V_{SB} applied as shown in Fig. 2.3, due to presence of V_{DS}, a wider depletion layer exists at drain.

At a distance y, V(y) and gate to channel voltage at that point is $V_G - V(y)$. If this voltage exceeds threshold voltage conducting channel is formed. The induced charge per unit area in the channel is at the point y.

$$Q_i(y) = Q_{SC}(y) - Q_B(y) \qquad (2.3)$$

where,

Q_{SC} = space charge layer charge per unit area.

$$Q_{SC} = -(V_G - \varphi_s)\, C_{ox}$$

$$Q_D = -\sqrt{(2q \epsilon_{si} N_A \varphi_s)}$$

Thus $Q_i(y) = -(V_{GS} - \varphi_s)\, C_{ox} + \sqrt{(2q \epsilon_{si} N_A \varphi_s)}$

Now surface band bending at a distance y is given as

$$\varphi_s = \varphi_{s_{inv}} + V(y)$$

Thus $$Q_i = -\left[V_{GS} - \left\{ V(y) + \varphi_{s_{inv}} \right\}\right] C_{ox}$$

$$+ \sqrt{2q \epsilon_{si} (V(y) N_A + \varphi_{s_{inv}})}$$

(2.4)

Assuming the conducting channel, to be homogeneous, so that ohms law is valid. The distance dR of a length dy of the channel

$$dR = \frac{dy}{W \cdot \mu_n |Q_i(y)|} \qquad (2.5)$$

where μn = average mobility of the electrons in the channel

W = channel width

The voltage drop along the length of the channel dy is given by

$$dV = I_D dR$$

$$= \frac{I_D}{W \cdot \mu_n |Q_i(y)|} dy$$

Substituting $Q_i(y)$ from (2.4) and integrating left side in voltage from V = 0 to V = V_{DS}, and Right side in length from y = 0 to y = L,

$$\int_0^{V_{DS}} dV = \frac{I_D}{W \mu_n} \left[\int_0^L -\left\{ V_{GS} - (V_{(y)} + \varphi_{s_{inv}}) \right\} C_{ox} \right.$$

$$\left. + [2q \epsilon_{si} N_A (V_{(y)} + \varphi_{s_{inv}})]^{1/2} \right]^{-1} dy.$$

$$I_D = \frac{W}{L} \mu_n C_{ox} \left\{ V_{DS} \left[V_{GS} - \varphi_{s_{inv}} - \frac{V_{DS}}{2} \right] - \frac{2}{3} k \left[(V_{DS} + \varphi_{s_{inv}})^{3/2} \right. \right.$$

$$\left. \left. - (\varphi_{s_{inv}})^{3/2} \right] \right\}$$

$$\text{with } k = \frac{\sqrt{(2q \epsilon_{si} N_A)}}{C_{ox}} \qquad (2.6)$$

For small V_{DS}, Eq. (2.6) is simplified as according to Shichman hodges model [5]:

$$I_D = \frac{W}{L} \mu_n C_{ox} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \qquad (2.7)$$

$$V_{DS} \leq V_{GS} - V_{th} \leq 0$$

where $V_{th} = \varphi_{s_{inv}} + \frac{\sqrt{(2q \epsilon_{si} N_A \varphi_{s_{inv}})}}{C_{ox}} + V_{FB}$

for linear region of operation.

And,

$$I_D = \frac{W}{2L} \mu_n C_{ox} \left[V_{GS} - V_{th} \right]^2 \qquad (2.8)$$

$$V_{DS} \geq V_{GS} - V_{th} \geq 0$$

2.5 FABRICATION PROCESS

The state of the art process sequence for fabrication of n channel MOSFET may be summarized in following steps [6].

a) A chemical vapour deposition (CVD) process deposits a thin layer of silicon nitride (Si_3N_4) on the entire wafer surface, silicon nitride is removed selectively and Boron is implanted in exposed areas to suppress unwanted conduction. Next a layer approx. 1μ thick of silicon dioxide (SiO_2) is deposi in these inactive or field regions.

b) The Si_3N_4 is removed and a clean thermal oxide about 0.1 micron thick is grown. Another CVD process deposits a layer

of polysilicon over the entire wafer. Next photolighography step defines the desired patterns for gate electrodes. Undesired poly is removed by chemical or plasma etching. An n type dopant is introduced to form source or drain by either thermal diffusion or ion-implantation . process. Later being necessary for self aligned source and drain structures.

c) Another CVD process deposits an insulating layer (SiO_2) over the entire wafer. A masking step for defining areas of contact followed by chemical or plasma etching selectively exposes bare silicon or poly in the contact areas.

d) Aluminium is deposited over the entire wafer by vacuume evaporation process. The next masking step patterns the Al as desired for connections to electrodes.

CHAPTER 3

THRESHOLD VOLTAGE OF SMALL GEOMETRY MOSFETS

3.1 INTRODUCTION

Recent progress in lithography has led to the fabrication of MOSFETs with small channel dimension. As the device size shrinks, two departures from long channel behaviour occur. These departures can be studied independently and are referred to as the short channel and narrow width effects. Threshold voltage is found to show wide variation with device down scaling. To evaluate overall device behaviour and performance, it is necessary to model the threshold voltage to accomodate such higher order effects.

In this chapter, first, effect of substrate bias on threshold voltage is considered. Two independent models have been presented for threshold voltage corresponding to short channel and narrow width effects. Finally all the three effects are combined to derive an expression for threshold voltage for small geometry MOSFETs. The models are based upon simple analytical approximations. The emphasis is mainly on the simplicity, speed and accuracy with a view to extending the MOS models for circuit simulator

To account the threshold voltage for graded substrate structure, a mathematical analysis has been presented to calculate the threshold shift.

3.2 EFFECT OF SUBSTRATE BIAS

The threshold voltage of a long channel MOSFET has been given in Chapter 2.

$$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{(2\epsilon_{si} qN_A(2\phi_f))}}{C_{ox}} \qquad (3.1)$$

Eq. (3.1) is threshold voltage expression without any terminal voltage applied and will have to be modified subsequently.

When an inversion layer is formed in MOS structure there is a P-N junction between the surface inversion region (channel) and the electrical neutral bulk material. Effect of substrate bias is then to increase the depletion layer thickness in the bulk.

Therefore depletion layer thickness on applying a substrate bias V_{SB},

$$X_d = \sqrt{\frac{2\epsilon_{si}(2\phi_f + V_{SB})}{qN_A}}$$

The threshold voltage expression (Eq. 3.1) modifies to

$$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{2 \epsilon_{si} q N_A (2\phi_f + V_{SB})}}{C_{ox}}$$

A factor K_s may be employed to denote the effect of substrate bias

$$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{2 \epsilon_{si} q N_A (2\phi_f)}}{C_{ox}} K_s \qquad (3.2a)$$

$$\text{With} \quad K_s = \sqrt{\left(1 + \frac{V_{SB}}{2\phi_f}\right)} \qquad (3.2b)$$

3.3 SHORT CHANNEL EFFECT

To achieve minimum feature length as the channel length is reduced, there is a considerable reduction in threshold voltage of MOSFET. The phenomenon, of short channel effect has been studied by a number of researchers. Yau [7], Lee [8], and Merckel [9] have provided closed form expression for threshold voltage based upon two dimensional charge sharing theory. In this section a simple model based on the same two dimensional charge sharing approximation has been given. The model includes drain biasing effect. Schematic diagram of a short channel MOSFET is shown in Fig. 3.1. Departure from long channel behaviour can be obtained by applying charge conservation principle to the region bounded by the metal gate and the bulk of the semiconductor.

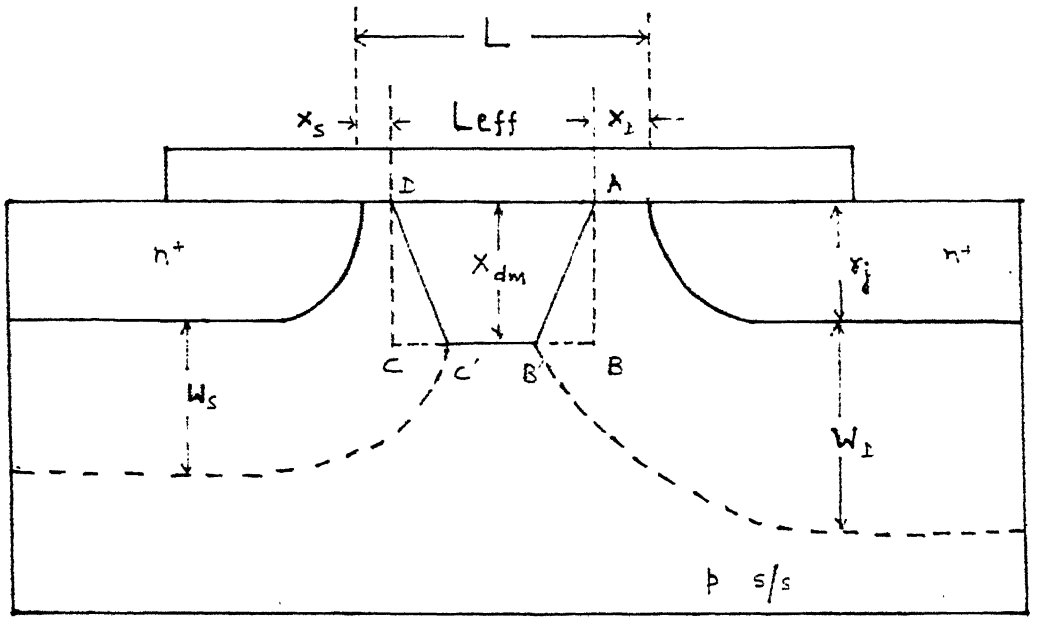


Fig. 3.1 Short Channel Schematic

$$Q_G + Q_{ox} + Q_n + Q_B = 0 \qquad (3.3a)$$

where,

Q_G = total charge on the gate

Q_{ox}= total effective charge at $Si-SiO_2$ interface

Q_n = total inversion layer charge of mobile electrons

Q_B = total bulk charge due to ionized impurity atoms in the depletion region.

Eq. (3.3a) may be expressed in terms of voltage, neglecting contribution due to Q_n at the onset of inversion.

$$V_G = V_{FB} + \varphi_s + \frac{Q_B}{C_{ox}LW}$$

The threshold voltage is given by setting $\varphi_s = 2\,\phi_f$,

$$V_{th} = V_{FB} + 2\phi_f + \frac{Q_B}{C_{ox}LW} \qquad (3.3b)$$

with L = channel length

W = channel width

For short channel devices the full effect of Q_B on the threshold voltage is reduced, as shown in Fig. 3.1. This is because some of the field lines originating from the source and drain terminates at bulk. For small drain voltages ($V_{DS} \leq$ 10 mV), the depletion layer charge under the gate may be treated as contained in trapezoid AB'C'D.

The effective bulk charge is then

$$Q_{B_{eff}} = K_L Q_B$$

where K_L is the charge sharing factor

$$K_L = \frac{\text{Area } (AB'C'D)}{\text{Area}(ABCD)}$$

Following the derivation given in Appendix A.

$$K_L = \frac{L-[(r_j+W_s)^2 - X_{dm}^2]^{1/2}-r_j-X_s}{L-2X_s} \qquad (3.4)$$

where

$$X_{dm} = \sqrt{\frac{2\epsilon_{si}(2\phi_f + V_{SB})}{qN_A}}$$

$$X_s = X_D = \sqrt{\frac{2\epsilon_{si}(V_{bi}-2\phi_f)}{qN_A}}$$

$W_s = W_D$, is obtained by solution of Poisson's equation, given in detail in Appendix A.

$$\frac{r_j^2-(W_s+r_j)^2}{2} + (W_s+r_j)^2 \ln\left(\frac{W_s+r_j}{r_j}\right) = 2\epsilon_{si} \times \frac{(V_{bi}+V_{SB})}{qN_A} \qquad (3.5)$$

For larger drain voltages, the depletion region near the drain expands further than that at the source. More charges under the gate now terminate at drain, as a result effective bulk charges under the gate decreases further. The charge sharing factor including the drain biasing effect modifies to (derivation in Appendix A):

$$K_L = \frac{2L-[(r_j+W_s)^2 - X_{dm}]^{1/2} - [(r_j+W_D)^2 - X_{dm}^2]^{1/2} - 2r_j - X_s - X_D}{2(L-X_s-X_D)} \tag{3.6}$$

With W_s given by equation (3.5), and W_D given by:

$$\frac{r_j^2-(r_j+W_D)^2}{2} + (r_j+W_D)^2 \ln\left[\frac{r_j+W_D}{r_j}\right] = \frac{2\epsilon_{si}(V_{DS}+V_{bi}+V_{SB})}{qN_A} \tag{3.7}$$

The equation of threshold voltage for short channel MOSFET is modified as:

$$V_{th} = V_{FB} + 2\phi_f + \frac{K_L Q_B}{C_{ox} WL}$$

where

$$Q_B = qN_A W X_{dm} \cdot L_{eff}$$

$$L_{eff} = L - X_s - X_D$$

$$V_{th} = V_{FB} + 2\phi_f + \frac{qN_A X_{dm} L_{eff}}{C_{ox} \cdot L} \times K_L \tag{3.9}$$

The factor K_L being given by equation (3.6).

In the above analysis, as the substrate bias is increased, the depth of the depletion region is also increased. Ref. to Fig. 3.1, point B' and C' coincides together for large V_{SB}, and the shape of the depletion region under the gate becomes triangular.

The charge sharing factor in this case simply becomes half as

$$K_L = \frac{\text{Area(ABE)}}{\text{Area(ABCD)}} = \frac{1}{2}$$

where E is the point where B' and C' coincides.

The depletion region width X_{dm}, now is

$$X'_{dm} = \frac{\left\{[2(2r_j+W_s+W_D)^2]^2-[(L-2r_j)^2-(r_j+W_s)^2-(r_j+W_D)^2]^2\right\}^{1/2}}{2(L+2r_j)} \qquad (3.10a)$$

The expression for threshold voltage assumes the form

$$V_{th} = V_{FB} + 2\phi_f + \frac{qN_A X'_{dm} L_{eff}}{2C_{ox}L} \qquad (3.10b)$$

Threshold voltage may be calculated using eq. (3.9).

For <100> silicon substrate ($Q_f = 1.4 \times 10^{-8}$ coulomb/cm^2) with aluminium gate ($\phi_{MS} = -0.92$ volts)

The flat band voltage

$$V_{FB} = -1.122 \text{ volts}$$

For long channel MOSFET (L=12 microns), with $N_A = 2 \times 10^{16}$/cc

$$X_{dm} = 3.04 \times 10^{-5} \text{ cms}$$

the threshold voltage

$$V_{th} = 0.259 \text{ volts}$$

If $V_{SB} = 1.0V$,

$V_{th} = 0.674$ volts.

The value of V_{th} will decrease and even become negative for short channel devices. For circuit application, however a large value of V_{th} is required.

In the present case we have added a voltage term equal to 1.0 volts. The origin of this term is related to ion-implantation with delta function approximation. The details are discussed in Section 3.5.

With this modification, theoretical plots of threshold voltage versus channel length have been given in Figs. 3.2 to 3.4 , with drain voltage, substrate voltage and oxide thickness as parameters.

A comparison between various models has been given in Fig. 3.5.

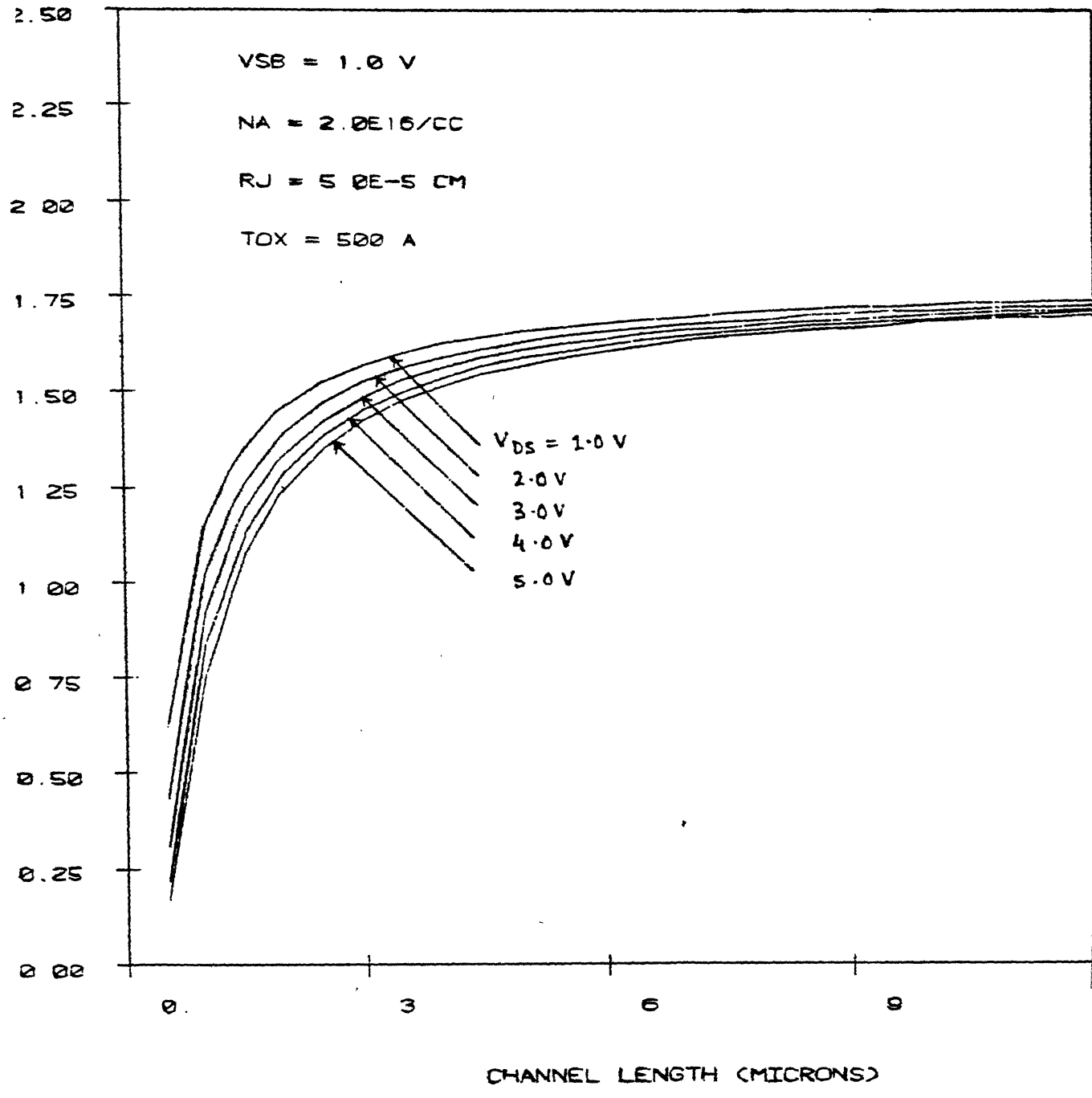

2.50
2.25
2 00
1.75
1.50
1 25
1 00
0 75
0.50
0.25
0 00
VSB = 1.0 V
NA = 2.0E16/CC
RJ = 5 0E-5 CM
TOX = 500 A
VDS = 1·0 V
2·0 V
3·0 V
4·0 V
5·0 V
0.
3
6
9
CHANNEL LENGTH (MICRONS)

Fig. 3.2

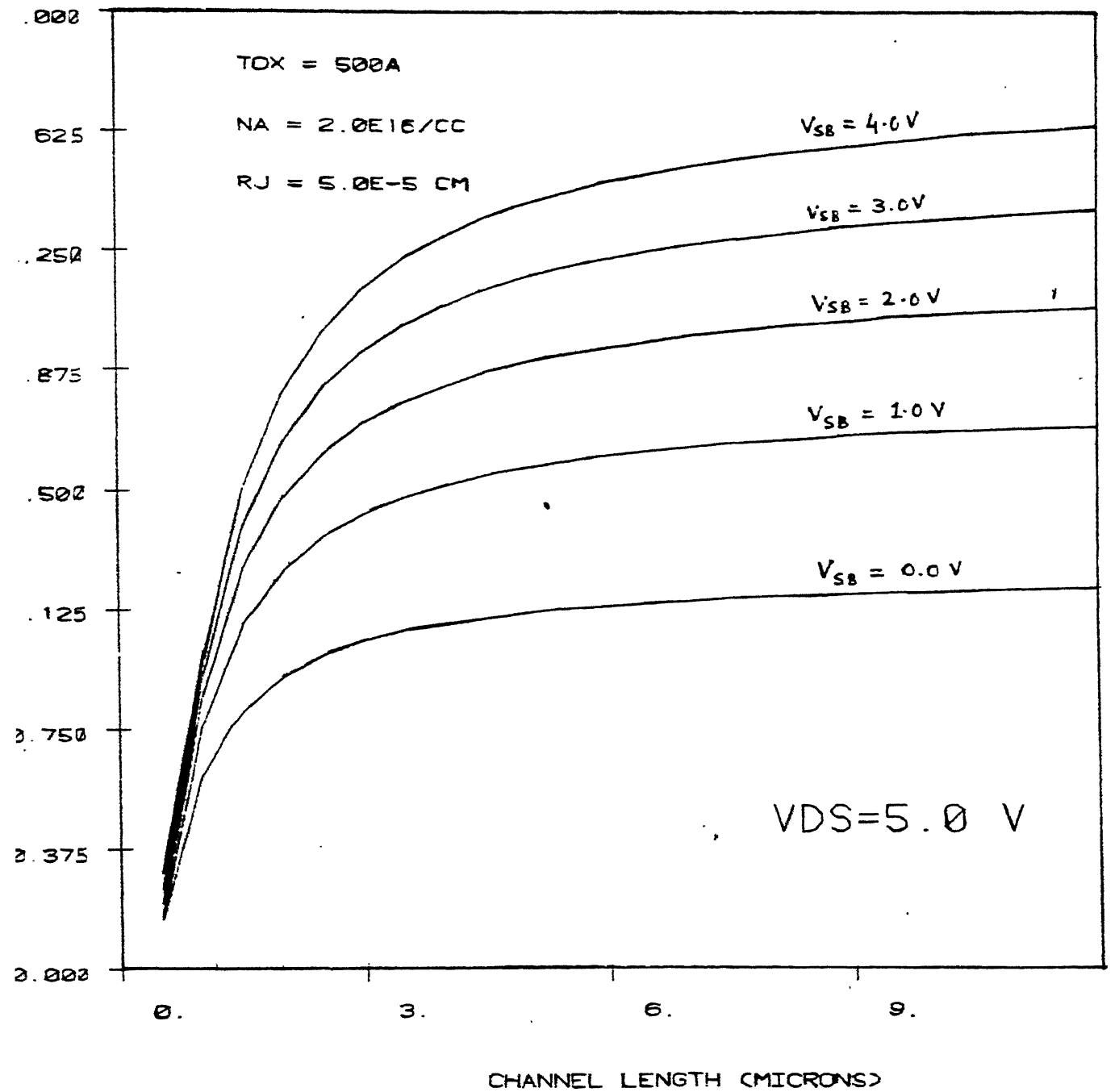

.000
625
.250
.875
.500
.125
3.750
3.375
3.000
TOX = 500A
NA = 2.0E16/CC
RJ = 5.0E-5 CM
VSB = 4.0 V
VSB = 3.0V
VSB = 2.0 V
VSB = 1.0 V
VSB = 0.0 V
VDS=5.0 V
0.
3.
6.
9.
CHANNEL LENGTH (MICRONS)

Fig. 3.3

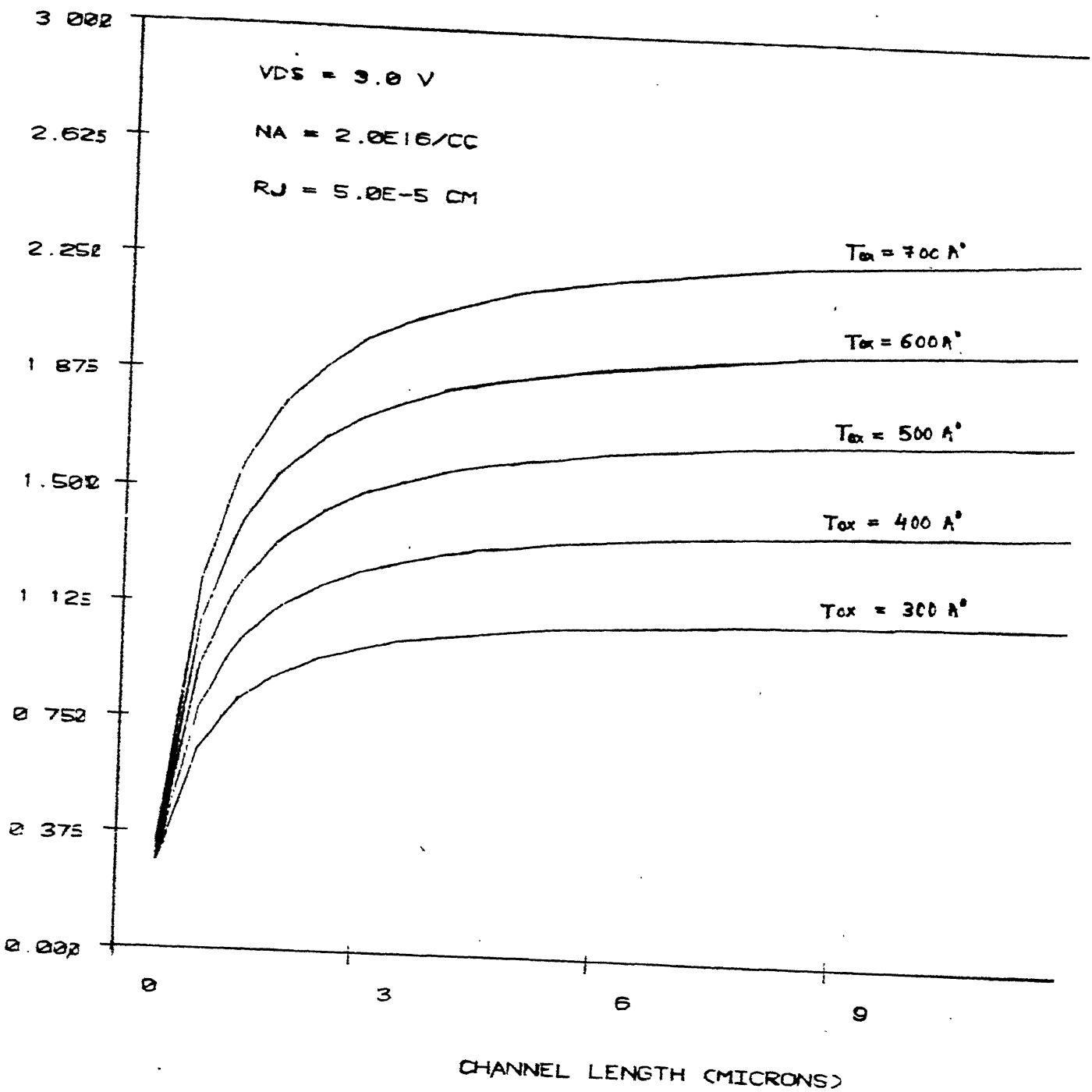
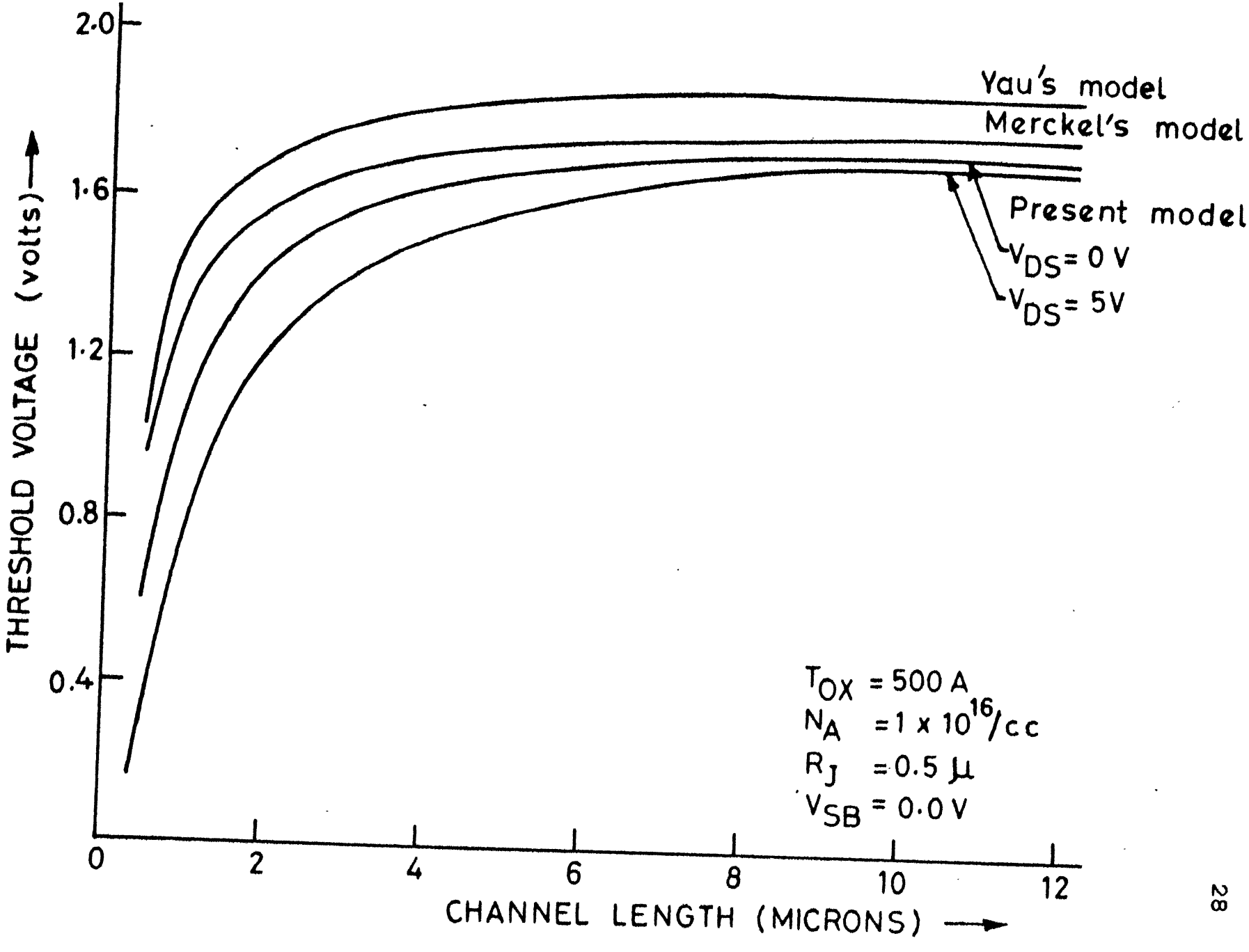

3 000
2.625
2.250
1 875
1.500
1 125
0 750
0 375
0.000
VDS = 3.0 V
NA = 2.0E16/CC
RJ = 5.0E-5 CM
Tox = 700 A°
Tox = 600 A°
Tox = 500 A°
Tox = 400 A°
Tox = 300 A°
0
3
6
9
CHANNEL LENGTH (MICRONS)

Fig. 3.4


2·0
1·6
1·2
0.8
0.4
THRESHOLD VOLTAGE (volts)
Yau's model
Merckel's model
Present model
V_{DS} = 0 V
V_{DS} = 5V
T_{OX} = 500 A
N_A = 1 x 10^{16}/cc
R_J = 0.5 μ
V_{SB} = 0.0 V
0
2
4
6
8
10
12
CHANNEL LENGTH (MICRONS)

3.4 NARROW WIDTH EFFECT

In contrast to the threshold voltage behaviour of short channel MOSFETs, narrow width devices show an increase in threshold voltage.

The cause of narrow width effect is chiefly attributed to the spreading of depletion layer charge under the thin oxide laterally [9]. With the reduction of the channel width of the MOSFET for VLSI applications, the effect assumes greater significance. An accurate expression for the threshold voltage should include process dependent considerations as well, which are described in this section.

Fig. 3.6 shows the device cross section looking from the width direction.

The gate overlaps the thick oxide on both the sides of thin gate oxide. The thick oxide on both sides does not change abruptly to the thin gate oxide, but is tapered and recessed. This results from fabrication process steps.

The narrow width effect, which increases the threshold voltage V_{th} as the width W is reduced, results from the charge stored under the thick oxide region and the transition of the electrostatic potential from deep to the shallow depletion region.

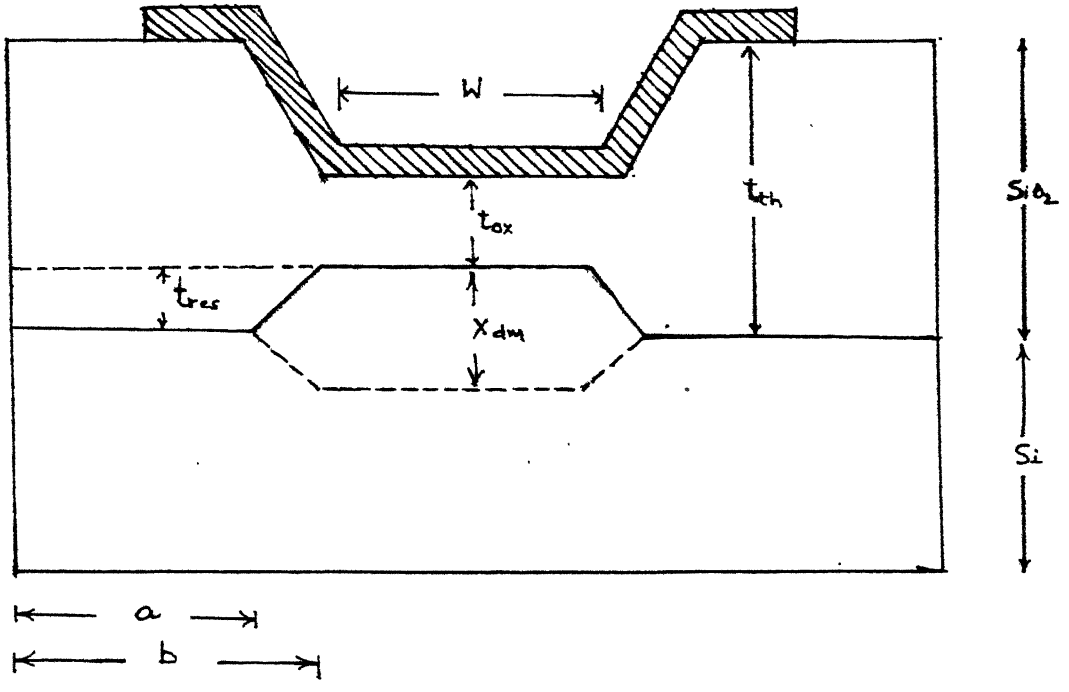


Fig. 3.6 Narrow Width Schematic

As W is reduced, the volume of the charge in the gate region is reduced, whereas in the tapered and thick oxide region the volume of the charge remains constant. This constant amount of charge becomes increasingly significant as W is reduced, and contributes to an increased threshold voltage.

Rewriting the threshold voltage expression for long channel MOSFET,

$$V_{th} = V_{FB} + 2\phi_f + \frac{Q_B'}{C_T'} \qquad (3.11)$$

here Q_B' is the total depletion charge induced and is given by

$$Q_B' = Q_B + 2Q_{TAP} + 2Q_{th} \quad .$$

where Q_B = total charge under thin oxide

Q_{TAP} = charge under tapered gate region

Q_{th} = charge under thick oxide region.

Q_B' is associated with a parallel combination of capacitances, the overall capacitance being

$$C_T' = C_{ox}' + 2C_{TAP} + 2\,C_{th}$$

Simple mathematical expressions are obtained for the various terms appeared above, the detailed derivations are given in Appendix A.

$$Q_{TAP} = \frac{qL\ X_{dm}\ N_a\ (b-a)}{2} \quad \text{Coulombs} \qquad (3.12a)$$

$$Q_B = qN_A\ X_{dm}\ WL \quad \text{Coulombs} \qquad (3.12b)$$

$$X_{dm} = \sqrt{\frac{2\ \epsilon_{si}(2\phi_f+V_{SB})}{qN_A}} \qquad (3.12c)$$

$$C'_{ox} = \frac{\epsilon_{ox}\ WL}{t_{ox}} \qquad (3.12d)$$

$$C_{TAP} = \frac{\epsilon_{ox} \cdot L}{\delta}\ \sqrt{d'}\ \ln\left[\frac{2d'b+f}{2d'a+f}\right] \qquad (3.12e)$$

where,

$$d' = 1+d^2 \qquad (3.13a)$$

$$d = \frac{t_{ox}+t_{res}-t_{th}}{(b-a)} \qquad (3.13b)$$

$$f = 2dy' - 2dg - 2z' \qquad (3.13c)$$

$$g = \frac{(t_{ox}+t_{res})a-t_{th} \cdot b}{(b-a)} \qquad (3.13d)$$

δ is the angle between capacitor plates given by

$$\delta = -\tan^{-1}\left[\frac{t_{res}}{(b-a)}\right] - \tan^{-1}\left[\frac{t_{th}-y'}{(z'-a)}\right] \qquad (3.13e)$$

Due to the higher threshold voltage, the depletion charge under thick oxide is small compared to that of Q_B and Q_{TAP}. Hence its contribution towards total depletion charge may be ignored without much loss of accuracy.

The modified threshold voltage expression incorporating the narrow width effect, may be written as

$$V_{th} = V_{FB} + 2\phi_f + \frac{Q_B + 2Q_{TAP}}{C'_{ox} + 2C_{TAP}}$$

$$= V_{FB} + 2\phi_f + \frac{Q_B}{C'_{ox}} \cdot K_W \qquad (3.14)$$

where $$K_W = \left(\frac{1 + 2Q_{TAP}/Q_B}{1 + 2C_{TAP}/C'_{ox}} \right) \qquad (3.15)$$

If a substrate bias is applied, the depletion region will spread into the substrate, but not under the thick and tapered oxide region. Therefore lateral spreading width under these areas is approximately the width at the conduction at zero substrate bias.

Threshold voltage calculations have been made using eq. (3.14) with following data.

t_{th} = 1000 A^{o}

t_{res} = 750 A^{o}

t_{ox} = 500 A^{o}

a = 2.0 microns

b = 2.5 microns

L = 25.0 microns

Theoretical plots of V_{th} versus channel width have been shown in Fig. (3.7), with doping density N_A as parameter.

3.5 SMALL GEOMETRY EFFECT

The short channel effect and narrow width effect are in contrast to eachsother. To predict the threshold voltage for short channel and narrow width devices, both the effects has to be combined. Yang [10] presented a theory to calculat threshold voltage of such devices by treating the effects independently.

For the present case, a general charge variation factor K is defined which is the combination of all the three effects described in this chapter.

Thus

$$V_{th} = V_{FB} + 2\phi_f + \sqrt{\frac{2\epsilon_{si} q N_A (2\phi_f)}{C_{ox}}}\ K \qquad (3.16)$$

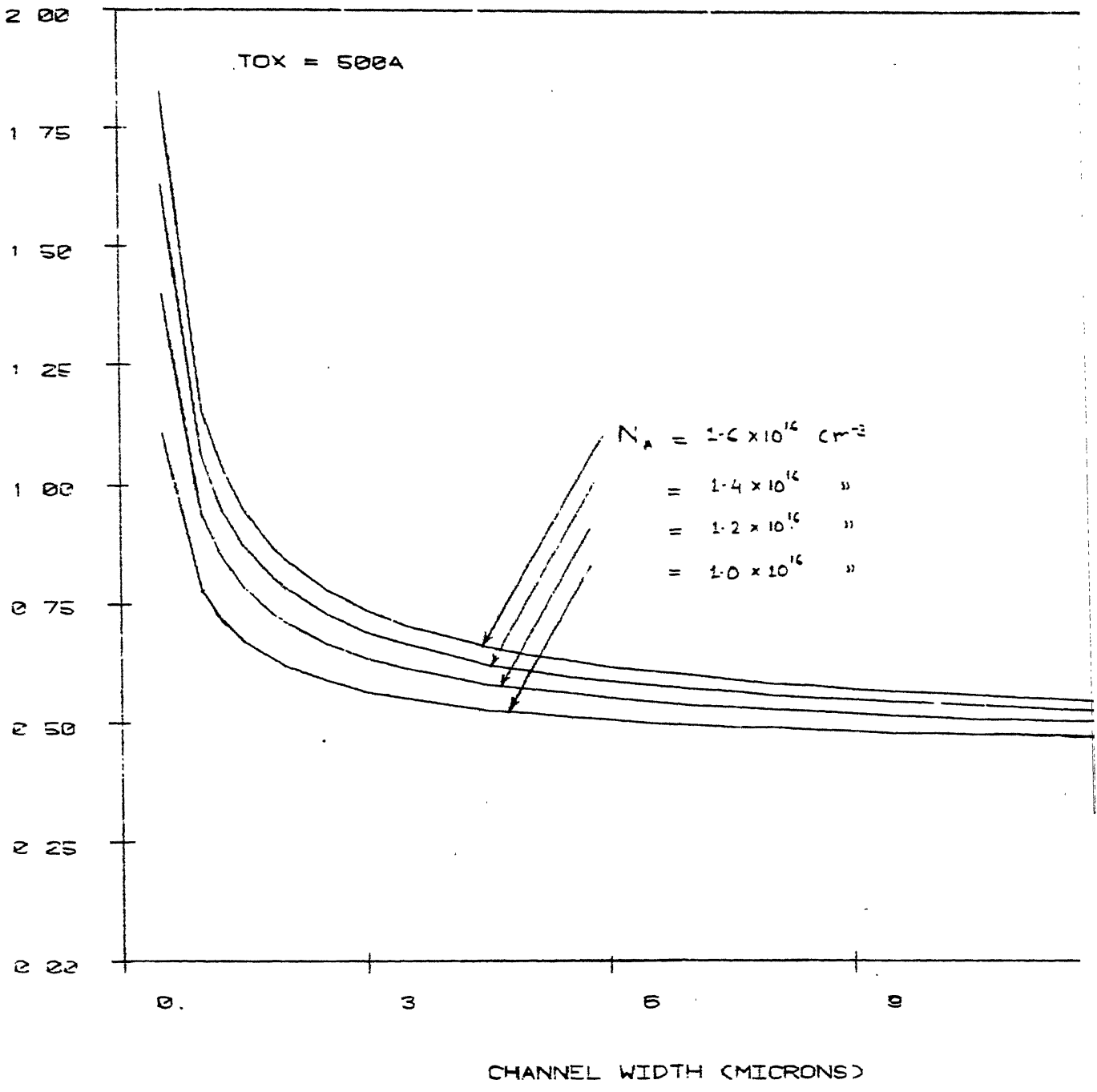

2 00
1 75
1 50
1 25
1 00
0 75
0 50
0 25
0 00
TOX = 500A
N_A = 1·6 x 10^16 cm^-3
= 1·4 x 10^16 »
= 1·2 x 10^16 »
= 1·0 x 10^16 »
0.
3
6
9
CHANNEL WIDTH (MICRONS)

Fig. 3.7

Each factor contributing towards K, may be calculated as and when required.

3.6 NON-UNIFORM DOPING

In first order analysis of MOSFET, the doping concentration in the channel is assumed to be constant. However in practical devices, the doping is generally non-uniform. Even for substrates that are initially uniformly doped, because of thermal oxidation impurity redistribution, non-uniformity takes place. Above all in modern MOS technology ion-implantation is used extensively to improve device performance, which causes nonuniform doping near the surface region of the channel.

In this section the effect of non-uniformly doped substrate on the threshold voltage is considered. The shift in the threshold voltage will affect the device and circuit performance.

Substrate profile after Boron ion-implantation is shown in Fig. 3.8. The original implant alters, after thermal annealing. For a first order result of threshold voltage, the annealed profile is approximated by a step function with a step depth X_s, equal to the sum of the

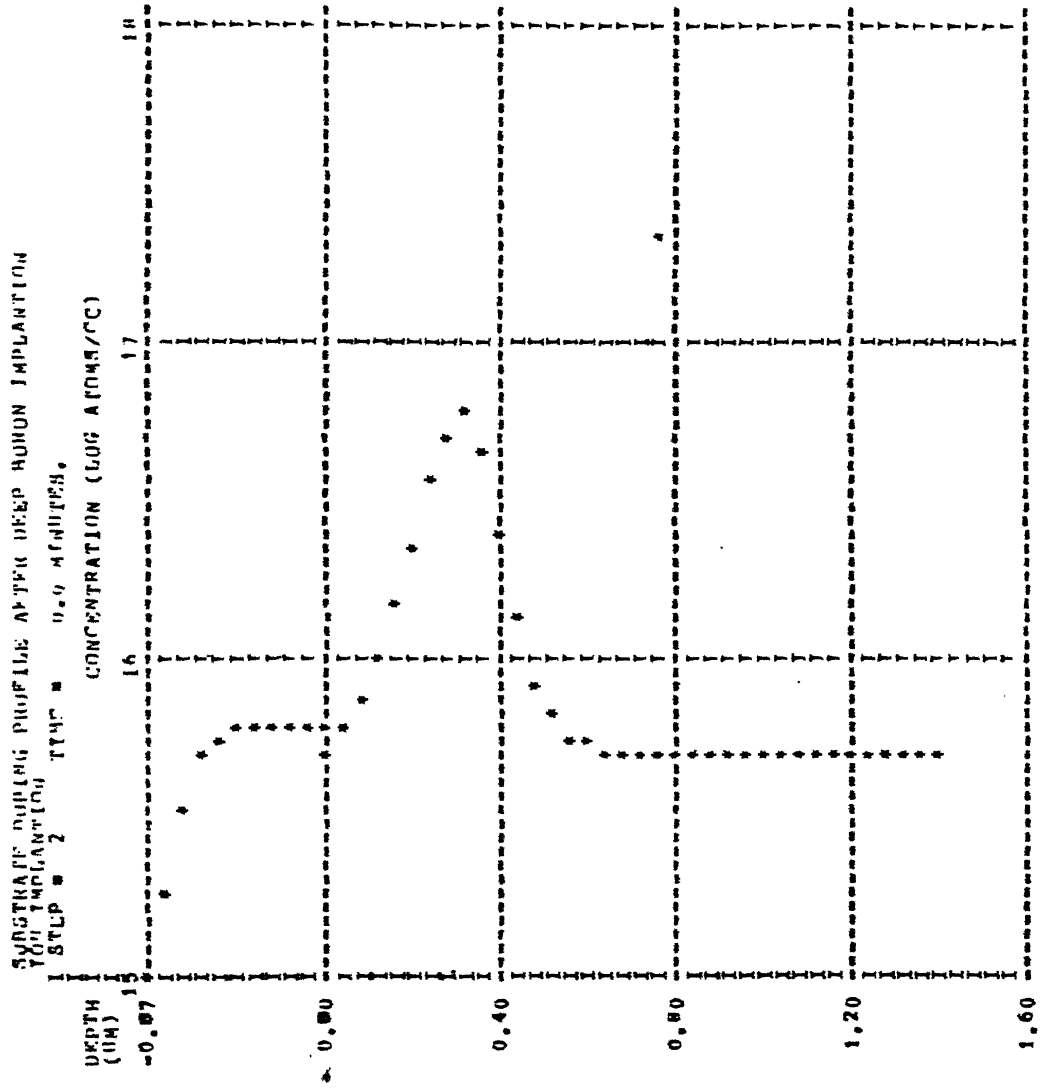


Fig. 3.8 Non-uniform Doping Profile

projected range and standard deviation of original profile (Fig. 3.9).

In this case the implant may be visualized as a delta function of negative charges (for Boron ion-implantation) localized at $Si-SiO_2$ interface. The charge is thus equivalent to a reduction in fixed oxide charges by an amount qD_I, where D_I is the implanted dose, and this term $\frac{qD_I}{C_{ox}} = 1.0$ volt has been taken in our calculations mentioned in Section 3.3.

$$D_I = \int_0^\infty (N_s - N_A)dx$$

N_s = Surface doping after annealing

N_A = Substrate doping

With the assumption that maximum depletion layer width X_{dm}, under heavy inversion is less than X_s, the surface region may be considered as a uniformly doped region with concentration N_s, the threshold voltage may be written as [11].

$$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{2 \epsilon_{si} q N_s (2\phi_f)}}{C_{ox}} + \frac{qD_I}{C_{ox}} \qquad (3.17)$$

In general the implanted dose of ions may lie partly in the oxide but the major part lies in the silicon. The portion of the dose in the depletion region alone is denoted as D_I.

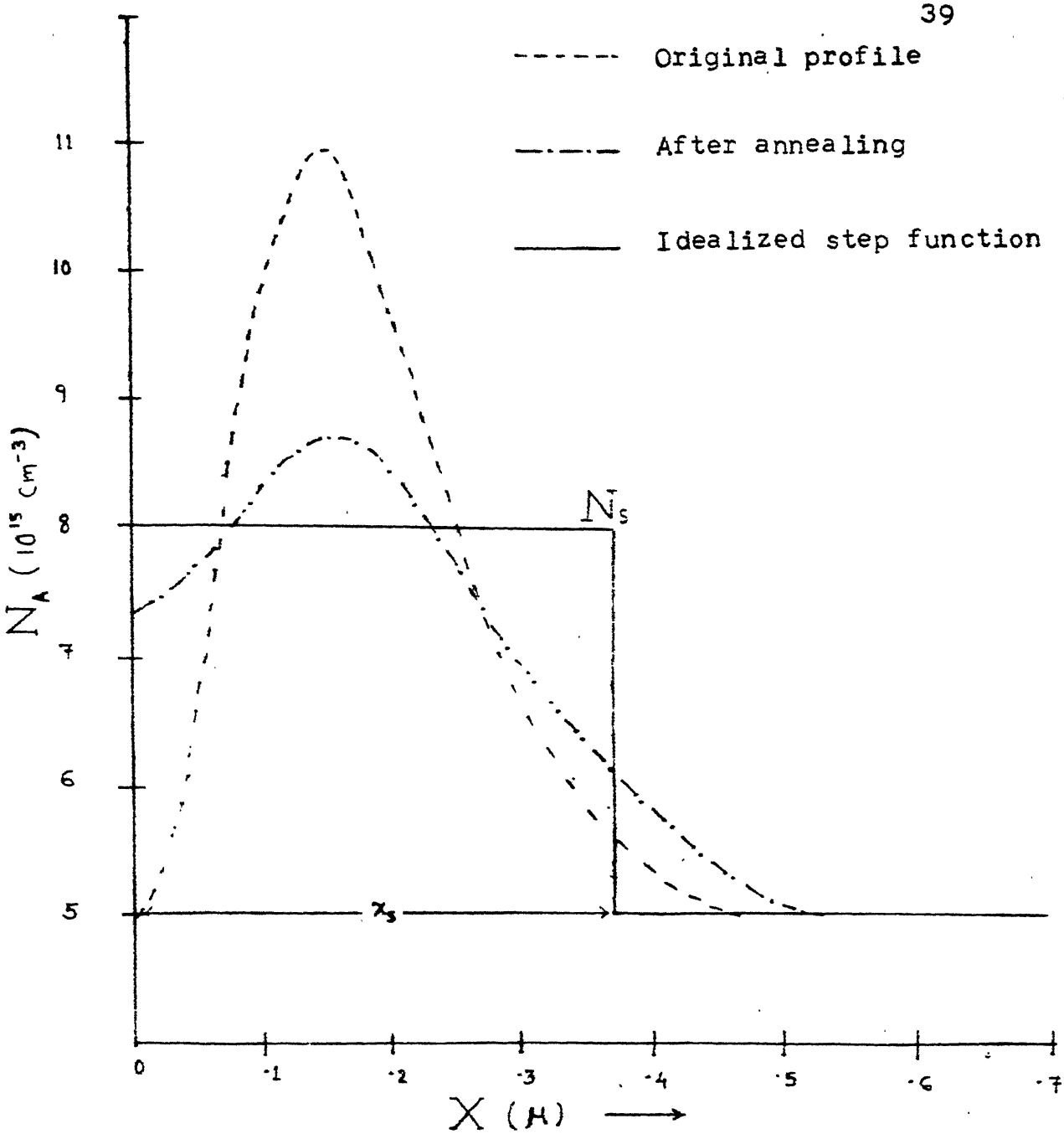


Fig. 3.9 Step Function Approximation

Relationship between surface band bending φ_s and gate voltage V_{GS} may be obtained by solution of poisson's equation [23]. This becomes necessary specially when

$$X_{dm} > X_s ,$$

The relationship may be written as:

$$V_{GS_I} = \varphi_s + \frac{a}{V_T}\left[\left(\frac{n_i}{N_A}\right)^2 \exp\left(-\frac{V_{SB}}{V_T}\right)\exp\left(\frac{\varphi_s}{V_T}\right)\right.$$

$$\left. + \left\{\left(\frac{\varphi_s}{V_T} - m_1 - 1\right)^{1/2} + \frac{m_o}{\sqrt{2}}\right\}^2\right]^{1/2} \qquad (3.18)$$

where,

$$a = \frac{\sqrt{2 \times \epsilon_{si} t_{ox}}}{\epsilon_{ox} \cdot L_D}$$

L_D is debye length

$$L_D = \sqrt{\frac{\epsilon_{si} V_T}{q N_A}}$$

$$V_T = \frac{KT}{q} \text{ volts.}$$

The parameters m_o, m_1 are the zero and first order moments of excess doping $(N(x)-N_A)$ of the non uniform surface defined as

$$m_o = \frac{1}{L_D} \int_o^{X_I} \left(\frac{N(x)}{N_A} - 1\right) dx \qquad (3.19)$$

$$m_1 = \frac{1}{L_D^2} \int_0^{X_I} \left(\frac{N(x)}{N_A} - 1 \right) x \, dx \qquad (3.19b)$$

(where X_I is depth of non-uniform region such that $N(X_I)=N_A$)

A similar relationship for unimplanted or uniformly dpoed substrate may be obtained from (3.18) putting $m_o=m_1=0$.

$$V_{GS_U} = \varphi_s + \frac{a}{V_T} \left[\left(\frac{h_i}{N_A}\right)^2 \exp\left(-\frac{V_{SB}}{V_T}\right) \exp\left(\frac{\varphi_s}{V_T}\right) + \left(\frac{\varphi_s}{V_T} - 1\right) \right]^{1/2} \qquad (3.20)$$

Under weak inversion condition, depletion layer charge per unit area for implanted subtrate is obtained as

$$\frac{Q_B}{C_{ox}} = \frac{a}{V_T} \left[\left(\frac{\varphi_s}{V_T} - m_1 - 1 \right)^{1/2} + \frac{m_o}{\sqrt{2}} \right] \qquad (3.21a)$$

Similarly for uniformly doped case

$$\frac{Q_B}{C_{ox}} = \frac{a}{V_T} \left(\frac{\varphi_s}{V_T} - 1 \right)^{1/2} \qquad (3.21b)$$

Minority carrier charge at inversion may then be obtained by substracting depletion layer charge from total charge.

$$\frac{q N_{inv}}{C_{ox}} = V_{GS} - \varphi_s - \frac{a}{V_T}\left[\left(\frac{\varphi_s}{V_T} - m_1 - 1\right)^{1/2} + m_o/\sqrt{2}\right] \tag{3.22}$$

There is a considerable disagreement among various researchers about the threshold voltage definition and the surface inversion criteria for the non uniformly doped substrates [12]-[13]. For the present case however the threshold voltage is defined as the gate voltage required for which minority carrier density equals depletion layer charge per unit area devided by depletion region thickness. The threshold voltage shift is predicted as difference in gate voltage needed to maintain the same minority carrier density, N_{inv} in the implanted and uniform structure.

Thus

$$\frac{q N_{inv}}{C_{ox}} = V_{G_I} - \varphi_{s_I} - \frac{a}{V_T}\left\{\left(\frac{\varphi_{s_I}}{V_T} - m_1 - 1\right)^{1/2} + \frac{m_o}{\sqrt{2}}\right\}$$

$$= V_{G_U} - \varphi_{s_U} - \frac{a}{V_T}\left(\frac{\varphi_{s_U}}{V_T} - 1\right)^{1/2} \tag{3.23}$$

Using above relationship, the threshold voltage shift ΔV_{th} may be written as

$$\Delta V_{th} = V_{G_I} - V_{G_U}$$

$$= (\varphi_{s_I} - \varphi_{s_U}) + \frac{a}{V_T}\left[\left(\frac{\varphi_{s_I}}{V_T} - m_1 - 1\right)^{1/2} + \frac{m_o}{\sqrt{2}} - \left(\frac{\varphi_{s_U}}{V_T} - 1\right)\right] \tag{3.24}$$

For a more realistic implanted profile, process simulator program SUPREM II [24] is used. It gives an accurate picture of the impurity concentration, obtained after a series of device fabrication steps. The threshold shift ΔV_{th} may be evaluated by calculating the parameters m_1 and m_o.

Considering a Gaussian profile implant of range R, straggle ΔR, and dose D_I.

$$N_{(x)} = \frac{D_I}{\sqrt{2\pi}\,\Delta R} \exp\left[- \left\{ \frac{X - (R-t_{ox})}{\sqrt{2}\,\Delta R} \right\}^2 \right]$$

Using equations (3.19a) and (3.19b)

$$m_o = \frac{D_I}{2N_A L_D}\left[1 + \operatorname{erf}\left(\frac{R-t_{ox}}{\sqrt{2}\,\Delta R} \right)\right] \qquad (3.25a)$$

$$m_1 = m_o \left\{ \left[\frac{(R-t_{ox})}{L_D} + \left(\frac{\Delta R}{L_D}\right)\left(\frac{2}{\pi}\right)^{1/2}\right] x \left[\frac{\exp[-(R-t_{ox})/(\sqrt{2}\,\Delta R)^2]}{1+\operatorname{erf}[(R-t_{ox})/\sqrt{2}\,\Delta R}\right] \right\} \qquad (3.25b)$$

where $\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_o^x \exp(-X^2)dx$

Surface potentials for implanted and uniformly doped substrate can be evaluated using following iteration scheme (derivation is in Appendix A).

$$\frac{\varphi_{s_I}^{I+1}}{V_T} = \frac{V_{SB}}{V_T} + 2 \ln \left(\frac{N_A}{n_i}\right) + \ln \left\{ \left[\frac{q N_{inv}}{V_T} / (a C_{ox}) \right]^2 + 2 \left[\frac{q N_{inv}}{V_T} / (a C_{ox}) \right] \left[\left(\frac{\varphi_s^I}{V_T} - m_1 - 1 \right)^{1/2} + \frac{m_o}{\sqrt{2}} \right] \right\} \quad (3.26a)$$

$$\frac{\varphi_{s_U}^{I+1}}{V_T} = \frac{V_{SB}}{V_T} + 2 \ln \left(\frac{N_A}{n_i} \right) + \ln \left\{ \left[\frac{q N_{inv}}{V_T} / (a C_{ox}) \right]^2 + 2 \left[\frac{q N_{inv}}{V_T} / (a C_{ox}) \right] \left(\frac{\varphi_s^I}{V_T} - 1 \right)^{1/2} \right\} \quad (3.26b)$$

Threshold shift due to implantation may be evaluated using (3.24) with (3.25a), (3.25b), (3.26a) and (3.26b).

As an illustrative example for a Gaussian implant with,

Range $R = 0.3$ micron,

Straggle $\Delta R = 0.08$ microns

Dose $D_I = 1 \times 10^{11}$/sq.cm

is used for a substrate with $N_A = 5 \times 10^{15}$/cc.

Following results were obtained for a substrate bias of 1.25 volts.

Threshold voltage shift

$$\Delta V_{th} = 0.413 \text{ volts}$$

A wide range of threshold voltage tailoring can thus be achieved by a choice of parameters R, ΔR, and D_I.

CHAPTER 4

OPERATING VOLTAGE LIMITATION DUE TO SCALING

4.1 INTRODUCTION

A wide range of operating voltage is applicable for large geometry MOSFETs in terms of gate and drain voltages. However as the device size decreases, a number of physical mechanism tends to reduce the upper limit for operating voltage. These mechanisms originate from high electric field due to device down scaling of oxide thickness and channel length. As the electric field is increased, the channel mobility becomes field dependent, when the field is increased further, carrier multiplication near the drain occurs leading to substrate current and parasitic bipolar transistor action. High field also causes injection of hot electrons into the oxide, leading to oxide charging and subsequent threshold voltage shift and transconductance degradation.

In this chapter, some of the effects, limiting the operating voltage has been considered. These include: punch through effect, breakdown voltage, hot carrier injection, oxide breakdown and mobility degradation. A brief theory

has been given in each case followed by a simple expression for describing the behaviour of the respective mechanism for small geometry MOSFET.

4.2 PUNCH THROUGH EFFECT

Among the aforesaid limiting factors for operating voltage of MOSFETs, punch through effect is significant as drain voltage onset of punch through goes down sharply with down scaling the channel length.

'Punch through' occurs when the drain space charge layer width reaches the space charge layer of the source. Upon occurence, shunt current flows in the bulk to augment the conduction current in the surface inversion region. This manifests itself as an increase in the output conductance of I_{DS} vs. V_{DS} transfer characteristics [25].

An accurate expression for drain voltage onset of punch through may be obtained by the solution of Poisson's equation in cylindrical coordinates.

The Poisson's equation in cylindrical coordinates can be written as

$$\frac{1}{r}\,\frac{\partial(r\,\partial V(r)/\partial r)}{\partial r} = \frac{q\,N_A}{\epsilon_{si}} \qquad (4.1)$$

Integrating with the boundary condition

$$-\left.\frac{\partial V(r)}{\partial r}\right|_{r=(r_j+W_D)} = 0$$

$$\frac{\partial V_{(r)}}{\partial r} = \frac{q\,N_A r}{2\,\epsilon_{si}} - \frac{q\,N_A}{2\,\epsilon_{si}}\,\frac{(r_j+W_D)^2}{r} \qquad (4.2)$$

Integrating within limits (r_j) to (r_j+W_D)

$$V_{bi} + V_{SB} + V_D = \frac{q\,N_A}{2\,\epsilon_{si}}\left(r_j - \frac{(r_j+W_D)^2}{2}\right) - \frac{q\,N_A(r_j+W_D)^2}{\epsilon_{si}} \times \ln\left(\frac{r_j}{r_j+W_D}\right)$$

$$V_D = \frac{q\,N_A}{2\,\epsilon_{si}}\left[(r_j+W_D)^2\left(\ln\left(\frac{r_j+W_D}{r_j}\right) - \frac{1}{2}\right) + \frac{r_j^2}{2}\right] - V_{bi} - V_{SB} \qquad (4.3)$$

with $W_D = L - W_s$ for punch through

where the source space charge depletion layer thickness W_s may be evaluated using eqn. (3.5),

As apparent from the expression itself to improve the punch through behaviour a high doping level is necessary but as this will affect breakdown voltage drastically, a trade off between punch through and breakdown voltage is useful. To

increase the punch through voltage single or double ion-implanted device structures can be made to increase the doping of the surface region.

4.3 THE OXIDE BREAKDOWN

The dielectric strength of SiO_2 is of the order of 700V/μ which limits the destructive gate breakdown voltage to above 7 volts/100 A^o of gate oxide thickness, thus gate oxide thickness of the order of 200 A^o are compatible with moderate power supply voltages. However care has to be taken that the technological steps (in particular, the high temperature treatments) do not effect the $Si-SiO_2$ (migration of the ions of the gate metal across the thin oxide layer).

4.4 THE BREAKDOWN VOLTAGE

Apart from punch through, the breakdown phenomena also determines the highest applicable voltage, and limits the speed and power handling capacity of discrete/integrated circuit device. Breakdown voltage is, therefore an important parameter in the design of the short channel MOS devices.

The drain breakdown voltage of a MOSFET is determined by the following two [15], phenomenon.

1. Avalanche breakdown of drain-substrate p-n junction caused by the high electric field between the gate and the drain.

2. I_D-V_D characteristic with a negative resistance (switch back) originating from lateral bipolar action which is induced by weak avalanche hole current.

The first one consists of simple p-n junction breakdown theory and has been studied by several authors [16]. The modification due to lateral bipolar action is more appropriate for small size (short channel) devices as will be apparent from further analysis.

The hole current generated by weak avalanche multiplication is injected into the substrate, so that some hole current can flow to the source. If drain voltage is low, most hole current flows out the substrate terminal. For large drain voltage, a substantial hole current can flow to the source, and the product of the current and substrate resistanc becomes large enough to forward bias the source substrate junction causing electron injection into the substrate. This injection leads to a parasitic n-p-n (source-substrate-drain) bipolar transistor action (Fig. 4.1). The breakdown voltage of MOSFET is then governed by the parasitic n-p-n transistor

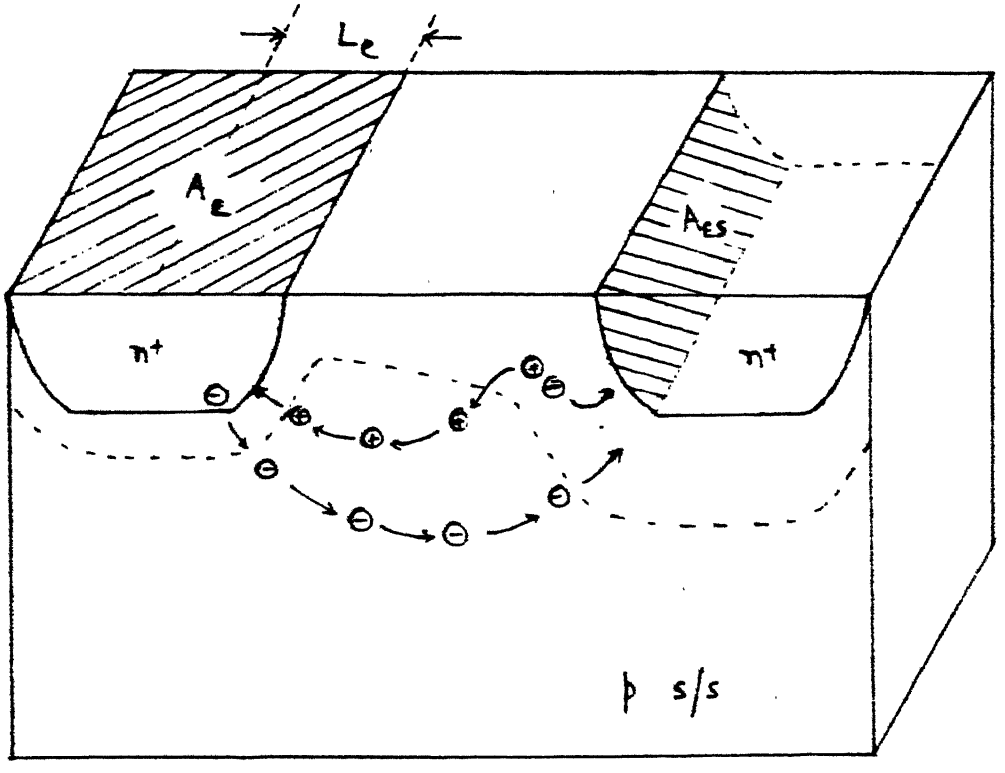


Fig. 4.1 Parasitic Bipolar Transistor Action

when floating base is assumed. From this point of view the following bipolar equations can be used to explain the switching phenomena.

The emitter (source) current

$$I_E = A_{E(eff)} \frac{q D_n n_p}{L_n} (e^{-V_{BE}/V_T} - 1) + A_{ES} \frac{q D_n n_p}{W_B} (e^{-V_{BE}/V_T} - 1) \quad (4.4)$$

The collector (drain) current

$$I_C \simeq A_{ES} \frac{q D_n n_p}{W_B} (e^{-V_{BE}/V_T} - 1)$$

where,

$A_{E(eff)}$ = effective emitter area

A_{ES} = emitter sidewall area

L_n = diffusion length of electrons in substrate

L_e = effective emitter length

W_B = the channel length L

Effective current gain

$$\alpha_{eff} = \frac{I_C}{I_E}$$

$$= \frac{A_{ES}/W_B}{\frac{A_{E(eff)}}{L_n} + \frac{A_{ES}}{W_B}}$$

$$= \frac{r_j/L}{L_e/L_n + r_j/L} \qquad (4.6)$$

Thus,

$$h_{FE_{eff}} = \frac{\alpha_{eff}}{1-\alpha_{eff}}$$

$$= \frac{L_n}{L_e}\left(\frac{r_j}{L}\right) \qquad (4.7)$$

The emitter collector breakdown voltage of a npn transistor is given by following equation (with open base).

$$BV_{CEO} = \frac{BV_j}{\sqrt{h_{FE_{eff}}}}$$

where BV_j is the pn junction breakdown voltage.

Corresponding source drain breakdown voltage then would be

$$BV_{DS} = \frac{BV_j}{\sqrt{\frac{L_n}{L_e}\left(\frac{r_j}{L}\right)}} \qquad (4.8)$$

JUNCTION CURVATURE EFFECT

Drain breakdown voltage BV_j is modified due to curvature of drain junction. Following [17], for cylindrical drain junction, the drain-substrate breakdown voltage is given by

$$V_{cy} = [\tfrac{1}{2} \quad (\eta^2+2\eta^{6/7})\ln(1+2\eta^{-8/7})-\eta^{6/7}]\times BV_j \qquad (4.9)$$

where $\eta = \frac{r_j}{W_m}$

W_m being depletion layer thickness at breakdown.

As it can be seen from the eqn. (4.8) the breakdown voltage is greatly reduced by decreasing the channel length L. This behaviour can be improved within a limit by using shallow source/drain diffusions and having larger values of L_e.

Theoretical plots of breakdown voltage versus channel length have been shown in Fig. 4.2, with the condition $L_e = r_j$, and diffusion length $L_n = 12.5\mu$.

4.5 HOT CARRIER EFFECT

Injection of hot carriers into the oxide causes performance variation during device operation. The physical mechanism is the emission of hot electrons from the silicon into silicon dioxide layer when applied voltage exceeds certain limits.

Hot electrons can originate from the channel current. According to the 'Lucky electron Model' [18], some of the electrons in the channel gain sufficient energy to surmount

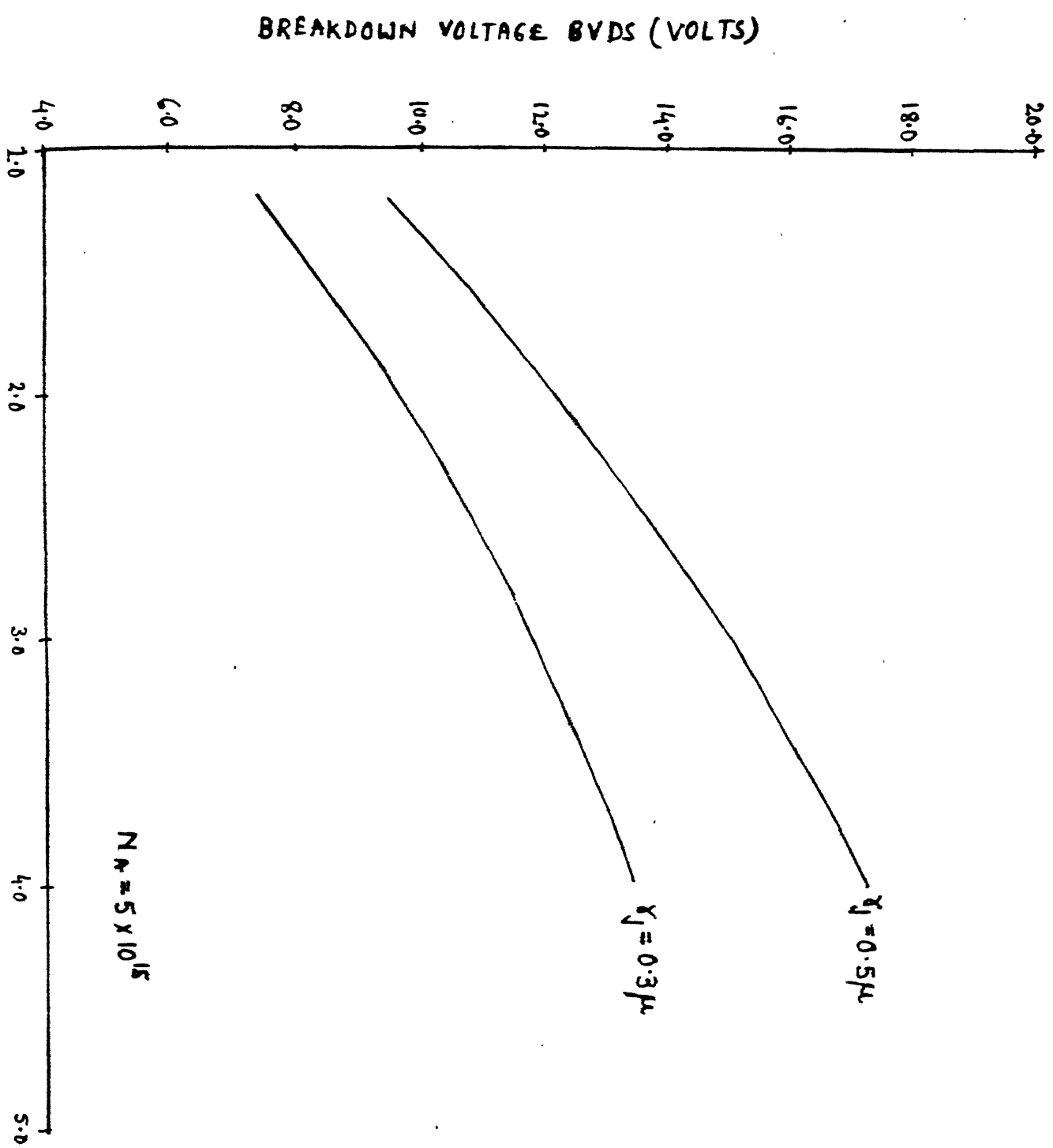

BREAKDOWN VOLTAGE BVDS (VOLTS)
4·0
6·0
8·0
10·0
12·0
14·0
16·0
18·0
20·0
1·0
2·0
3·0
4·0
5·0
N_A = 5 x 10^15
x_j = 0·3μ
x_j = 0·5μ

Fig. 4.2

$Si-SiO_2$ energy barrier (barrier height ≃ 3.1 eV) without suffering an energy losing collision. These electrons are injected into the SiO_2. This phenomena is known as channel hot electron effect or CHE.

The hot electrons can also be generated from substrate leakage current and is termed as substrate hot electron effect or SHE.

Trapping of the injected hot electrons in the gate insulator layer can cause instability in the form of trans-conductance degradation and threshold shift. Threshold shift can also occur from hot hole injection but this usually occurs only when drain is heavily avalanching.

In order to account for hot carrier injection and to understand guiding principles is optimizing device structure a deep insight into the mechanism is necessary. A brief discussion on gate current and channel current will reveal the nature of hot carrier emission.

The primary source of channel hot electron is channel current. As the voltage approaches drain breakdown voltage, avalanche multiplication due to thermal leakage current near the drain also supply hot electrons in the channel. Electrons moving from source to drain gain energy from high field near

the drain and become 'heated electron gas'. A small fraction of such electrons surmount the $Si-SiO_2$ energy barrier and are injected into the oxide. Under the condition $V_{GS}=V_{DS}$ 'lucky electrons' proves to be dominant than hot electrons caused by avalanche multiplication. Thus the electron gate current expected to be

$$I_G^e \alpha I_s \exp\left(-\frac{\phi_e}{kT_e}\right) \qquad (4.10)$$

where,

I_s = channel current

ϕ_e = barrier height

T_e = electron temp.

The hole gate current I_G^h is generated from hot holes due to 'impact ionization'. Most of the hole current, which are generated from avalanche multiplication near the drain under the bias $V_{GS} < V_{DS}$, flow towards the substrate as hole current. Only a small fraction of hole current is injected as hole gate current.

Following the 'quasi thermal equilibrium approximation' [19] the gate current may simply be obtained by integrating Richardson's expression for the thermionic current.

$$J_G = qn_s \left(\frac{KT_e}{2\pi m^*}\right)^{1/2} \exp\left(-\frac{\phi_e}{kT_e}\right) \qquad (4.11)$$

where,

m^* = effective mass of electron

n_s = surface electron density.

The electron temperature T_e, can be obtained by using following expression [19].

$$T_e = \frac{2q}{5K} \int_o^\infty E_y\,(y-u)\exp\left(-\frac{3u}{5\,\tau_e V_s}\right)du. \qquad (4.12)$$

where,

τ_e = electron relaxation time

E_y = component of the electric field

V_s = saturation velocity of electron.

An important assumption is that velocity V is parallel to the surface.

For the small length devices the SHE voltage limits are much larger than CHE. As such the modelling of SHE is not much important. However substrate current is of the form

$$I_{sub} \alpha \exp(-b/V_{DS}) \qquad (4.13)$$

where b is a constant.

Device Degradation:

The hot carrier injection into the gate oxide is known for imposing, among the severest limitation on the miniaturization of MOSFET in VLSI, This is because the part of the carriers trapped in the oxide cause long term device degradation. The initial damage appears a transconductance degradation, although very severe channel hot electron stress generally results in a combination of transconductance degradation and real threshold voltage shift. Long term operation of the device is seriously affected by oxide charging, because the charging continues to increase with time during device operation. As a result of this cumulative degradation, oxide charging limits the maximum voltage levels that can be applied for a given specific device life time.

Minimization of hot carrier effect:

Fine line patterning techniques such as electron beam lithography and reactive ion etching utilize radiative process steps. These process steps known to introduce charged as well as neutral electron traps in the oxide, which enhances device degradation due to hot carrier injection. Experiments shows that [32] threshold shifts due to channel hot electron injection in devices fabricated by electron beam lithography is much more enhanced than device prepared by optical lithography.

A number of MOSFET structures were suggested as 'Hot carrier resistant' structures. These include As-P($n^+ - n^-$) double diffused drain, drain offset gate and burried channel devices. The basic guiding principles for minimizing hot carrier generation are:

1. Use of a graded drain junction for reducing electric field.
2. Use of an offset gate for separating the gate electrode from the localized peak of the electric field.

4.6 CARRIER MOBILITY

One of the most important quantity which determines the electrical behaviour of MOSFET is carrier mobility. The carrier mobility varies significantly in small geometry MOSFETs due to higher internal electric fields existing in such devices. An exact model of carrier mobility is worthwhile since it determines the current levels in MOSFET.

A brief theory for carrier mobility has been given including various influencing parameters on mobility. Later in this section a simple model describing exact mobility behaviour in MOSFET has been given.

Mobility depends on factors such as the electric field strength, doping concentrations and the temperature.

However the variations depends upon the band structure of the semiconductor and the scattering mechanism which exists within a given device. The carrier mobility can be expressed by following simple relation

$$\mu = \frac{q \langle \tau_c \rangle}{m^*} \qquad (4.14)$$

where,

τ_c = average carrier life time

m^* = effective mass of the carrier.

The effective mass m* being a dependent on the band structure of the device.

The impurity doping concentration and temperature influence on carrier mobility is obvious as due to their impact on scattering processes.

Few important scattering mechanisms are as follows:

1. Coulomb Scattering:

Occurs due to ionized impurities and most important of all processes at low velocities. Thus dominant at low temperature and high doping density mobility in this case [20]

$$\mu_i = \frac{(m^*)^{-1/2} . T^{3/2}}{N_I} \qquad (4.15)$$

N_I = Ionized impurity density

2. Scattering due to Lattice Vibrations:

This process is dominant at high temperature. The process incluces optical and acoustic phenon scattering. For non-polar semiconductor like silicon the acoustic phenon scattering is more important, and the resulting mobility [21]:

$$\mu_L = (m^*)^{-5/2}\ {}_T{}^{-3/2} \qquad (4.16)$$

3. Ionized Impurity Scattering:

Results due to electron-electron and hole-hole interaction.

4. Neutral Impurity Collision:

Results due to presence of neutral impurity atom having size different than host lattice atom causing a disturbance in periodic potential.

5. Defect Related Imperfections in Lattice.

The other factors includes the radiation induced charges and interfacial states in the oxide degrading the surface mobility characteristics.

All the above mentioned mechanisms contributes together to produce overall mobility behaviour, however the exact value is determined by the operating temperature and impurity level. In ordinary conditions the net mobility is given by

$$\mu = \left(\frac{1}{\mu_L} + \frac{1}{\mu_I}\right)^{-1} \qquad (4.17)$$

The electric field dependence comes about because of the changes in the momentum distribution among the carriers. This effectively transfers the carriers to different positions along the energy momentum curves thereby changing their effective mass. Solving carrier velocity distribution function, starting from the boltzman transport equation, following relationship for the mobility results.

$$\mu = \frac{q \langle v^2 \tau_c \rangle}{m^* \langle v^2 \rangle} \qquad (4.18)$$

Mobility behaviour in MOSFET:

As the current in MOSFET flows only in the inversion layer, mobility and drift velocity are expected to be influenced by the thickness of the inversion layer. From both field effect and hall effect it has been found that the free carrier mobility depends on the normal field i.e. the field perpendicular to the direction of current flow however it has been found experimentally [11] that it is not a function of surface processing or doping density in the range $N_A < 10^{17}$ cm^{-3}. At a given temperature mobility decreases with increasing effective

transverse field, this observation is well supported by classical theory for surface scattering in a linear potential well.

Another observed fact is at high lateral fields the mobility also decreases due to velocity saturation, when the longitudinal field increases, eventually velocity saturation occurs similar to bulk silicon. For a given normal field E_x, the velocity is proportional to E_y with a proportional constant equal to mobility. However as E_y increases, the velocity tends to saturate.

A mobility model corresponding to the experimentally calculated values thus proposed as

$$\mu = \frac{\mu_o}{(1+\theta_G(V_{GS}-V_{TO}))(1+\theta_D V_{DS})} \qquad (4.19)$$

where,

μ_o = surface mobility under zero field

θ_G = Coeff. for normal field dependence

θ_D = Coeff. for lateral field dependence

V_{TO} = threshold voltage with zero substrate voltage.

For short channel MOSFETs the factors modify as follows:

a) Carrier Mobility under Zero Field:

Based on a number of experimentally verified results [22], the mobility under zero fields is modified as

$$\mu_o = \frac{\mu_B}{2}$$

where μ_B is bulk carrier mobility.

b) The Coefficient θ_G:

This parameter is a function of oxide thickness and is given as

$$\theta_G = a_i C_{ox}$$

where,

a_i is a constant such that

$a_i = 10^6$ cm^2/coul. for p channel device

$10^7 < a_i < 10^6$ cm^2/coul. for n channel device.

The Coefficient θ_D:

This parameter is a function of channel length and is given by a relation

$$\theta_D = (L\, E_o)^{-1}$$

where,

E_o = Longitudinal critical field

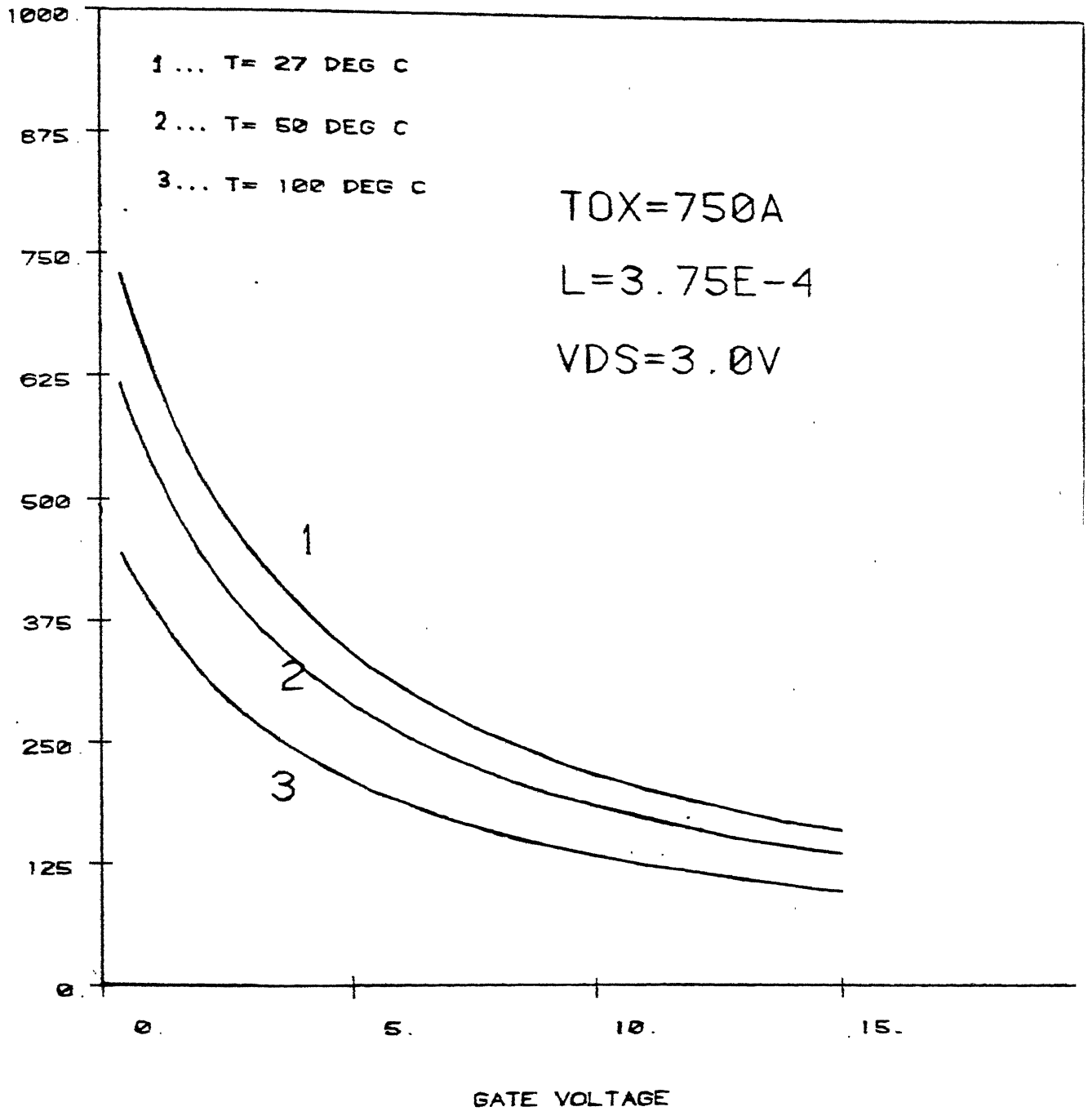

1000
875
750
625
500
375
250
125
0
1 ... T= 27 DEG C
2 ... T= 50 DEG C
3 ... T= 100 DEG C
TOX=750A
L=3.75E-4
VDS=3.0V
1
2
3
0
5.
10.
15.
GATE VOLTAGE

Fig. 4.3

For p channel device, $E_o \geq 10$ V/μ

For n channel devices $E_o \leq 3$V/μ

Using the relationships

$$\mu = \frac{\mu_B/2}{(1+a_i C_{ox}(V_{GS}-V_{TO}))(1+\frac{V_{DS}}{LE_o})} \qquad (4.20)$$

Carrier mobility has a different temperature dependence at different ranges. However for practical purposes a $T^{-2.4}$ variation can be assumed for n type silicon devices.

Theoretical plots of mobility variation with gate voltage have been given for three different temperature in Fig. 4.3, with following data:

μ_B = 1500 cm^2/volts-sec.

a_i = 5×10^6 cm^2/coul.

E_o = 2.5 volts/micron

L = 3.75 microns

V_{DS} = 3.0 volts

and T_{ox} = 750 A^o.

CHAPTER 5

CONDUCTION IN MOSFET AT BELOW AND ABOVE THRESHOLD

5.1 INTRODUCTION

State of the art MOS LSI, like random access memories (dynamic and static), microprocessors, read only memories and shift registers use MOSFET with channel length 1 to 6 microns. It is therefore, important to predict the conduction behaviour of MOSFET correctly for these range of dimensions. The binary logic states for the MOSFETs are defined as follows:

LOGIC STATE	DEVICE OPERATION	NODE VOLTAGE
Zero	OFF	$V_{GS} < V_{th}$
One	ON	$V_{GS} > V_{th}$

However there is a finite drain current even at $V_{GS} < V_{th}$. This subthreshold current or weak inversion current is important. In high performance dynamic RAMS, the magnitude of subthreshold current results in poor refresh times, pattern sensitivity and poor long cycle operation. Magnitude of subthreshold current becomes even more significant as channel length reduces. In the following sections a simple device model for subthreshold conductionis given for short

channel MOSFETs based on analytical approach and is more suited for computer aided LSI design.

The original long channel current voltage relationship has been modified for small geometry MOSFETs. All the small geometry effects discussed in the previous sections have been accomodated in the present model.

5.2 SUBTHRESHOLD CONDUCTION

For the gate voltage below threshold voltage, the semiconductor surface is in weak inversion. Corresponding drain current i.e. subthreshold current behaviour is, obviously totally different from that of above threshold. Subthreshold current for long channel MOSFETs has been well characterized by a number of researchers [26]-[28], but published work is limited for short channel MOSFETs. Literatu available for short channel case, mostly uses numerical methods and fitting parameter techniques [29]-[30]. These parameters often have to be re-evaluated for different devices or different ranges of values and therefore not suited well for circuit analysis or statistical modelling. A complete analytical model also provide better insight into the operation of device. In the present section one such analytical model has been described.

The drain current I_{DS} consists of two components namely drift and diffusion current.

$$I_{DS} = I_{drift} + I_{diff} \qquad (5.1)$$

I_{drift} is dominant only if the gate is biased above threshold and if $V_{DS} \neq 0$, while I_{diff} is present with a carrier concentration gradient along the channel. The drain current in weak inversion is dominated by diffusion and is derived in the same way as the collector current in bipolar transistor with a homogeneous base doping.

Considering the MOSFET as an n-p-n (source-substrate-drain) bipolar transistor,

$$I_{DS} = -q\ A\ D_n\ \frac{dn}{dy} \qquad (5.2)$$

where,

A = cross section of current flow

D_n = diffusion constant of electrons in the channel

n = density of electrons in the channel.

Since current is diffusion current and thus distribution of free carriers along the channel is given by the solution of following continuty equation:

$$\frac{d^2 \Delta n}{dy^2} - \frac{\Delta n}{L_n^2} = 0 \qquad (5.3)$$

where,

$\Delta n = n_s - n$

L_n = diffusion length of electrons in the channel

n_s being the electron density at source depletion layer edge.

Eq. (5.3) may be solved using following boundary conditions.

$$\Delta n|_{y_s} = 0 \qquad (5.4)$$

$$\Delta n|_{L-y_D} = n_s[1-\exp(-\frac{qV_{DS}}{kT})] \qquad (5.5)$$

where y_s and y_D are the source and drain depletion layer thicknesses.

From the solution of eq. (5.3), the free carrier density variation Δn along the channel at the surface is given by

$$\Delta n = n_s(1-e^{-qV_{DS}/kT}) \frac{\sin h(\frac{y-y_s}{L_n})}{\sin h(\frac{L-y_s-y_D}{L_n})} \qquad (5.6)$$

electron density at source depletion layer edge, n_s is given by

$$n_s = n_G \, e^{q \varphi_s / kT}$$

where,

n_G = electron density at gate depletion layer edge

φ_s = surface potential

$n_G = n_i \, e^{-q \phi_f / kT}$

The Surface Potential φ_s

Using the geometrical approximation for short channel devices as in Chapter 3, with refer to Fig. 3.1, the voltage applied at gate may be related to surface potential as follows:

$$V_{GS} = V_{FB} + \phi_s + \sqrt{(2 \epsilon_{si} q N_A x \varphi_s)} F \qquad (5.7)$$

The geometrical charge sharing factor F has been obtained by same trapezoidal approximation, however, to obtain a simple close form expression for φ_s, the junction depth r_j is assumed to be large, and F assumes the form

$$F = \left[1 + \frac{(L - W_s - W_D)}{(L - y_s - y_D)} \right] \qquad (5.8)$$

where W_s and W_D are source and drain depletion layer width, and

$$y_s = \sqrt{\frac{2\epsilon_{si}(V_{bi}-\varphi_s)}{qN_A}} \qquad (5.9a)$$

$$y_D = \sqrt{\frac{2\epsilon_{si}(V_{in}-\varphi_s+V_{DS})}{qN_A}} \qquad (5.9b)$$

Now since φ_s, for subthreshold region varies over a small range (0.3 - 0.6), an average value of φ_s may be used in square root terms in eq. (5.9), due to its weak dependence on φ_s, For present case average value of φ_s is taken as $\varphi_{s_{av}} = 0.45V$.

Using these assumptions, the surface potential φ_s becomes, (solving eqn. (5.7)),

$$\varphi_s = (V_{GS}-V_{FB})+V' - \sqrt{((V_{GS}-V_{FB}+V')^2-(V_{GS}-V_{FB})^2+2V'\cdot V_{SB})} \qquad (5.10)$$

with

$$V' = \frac{\epsilon_{si} qN_A F^2}{C_{ox}^2}$$

with F given by eq. (5.8).

Cross Section of Current Flow:

Cross section of current flow A may be written as

$$A = W \times X_i$$

where X_i = channel thickness.

Expression for X_i is derived in the appendix B, and is

$$X_i = \sqrt{\frac{\epsilon_{si} \times kT}{2q^2 N_A (\frac{q}{kT}(\varphi_s + V_{SB}) + 1)}} \qquad (5.11)$$

Subthreshold current is then determined at the edge of drain depletion region

$$I_{DS} = qD_n W X_i \left.\frac{d\,\Delta n}{dy}\right|_{y=L-y_D}$$

Using equation (5.6),

$$I_{DS} = \frac{q\,WD_n}{L_n} X_i \cdot n_s \cdot \frac{1}{\tanh(\frac{L-y_s-y_D}{L_n})} (1-e^{-qV_{DS}/KT}) \qquad (5.12)$$

Now for short channel devices

$$\tanh(\frac{L-y_s-y_D}{L_n}) = \frac{L-y_s-y_D}{L_n}$$

since normally $L_n > 10\ \mu$

drain subthreshold current is then

$$I_{DS} = \frac{qWD_n X_i}{(L-y_s-y_D)} n_i e^{-q\,\phi_f/KT} [1-e^{-qV_{DS}/KT}] \times \exp[\frac{q\varphi_s}{KT}] \qquad (5.13)$$

I_{DS} vs. V_{DS} characteristics -

i) For small drain voltage ($\sim$ few $\frac{KT}{q}$) the value of φ_s is taken as constant since dependence of V_{DS} on φ_s comes only through the charge sharing factor F. The I_{DS} varies exponentially with V_{DS}.

ii) For voltages $V_{DS} > 3. \frac{KT}{q}$, the exponential term in V_{DS}, rapidly vanishes, and variation of y_d and φ_s dominates I_{ds}. Thus in this range, leaving the exponential term in V_{DS},

$$I_{DS} = \frac{qW\ D_n\ X_i}{(L-y_s-y_D)}\ e^{-q\phi_f/KT}\ \exp\left[\frac{q\varphi_s}{KT}\right] \qquad (5.14)$$

Eq. (5.14) shows cross product of drain and substrate voltage, hence as the substrate bias is increased, the dependence of current upon drain voltage will also increase. However, the dependence of the current on drain voltage will be a function of oxide thickness and substrate doping.

With increase in drain voltage V_{DS}, drain depletion layer width y_D increases and as predicted by eq. (5.14) drain current also increases for short channel devices the increase in drain current is much more prominent, and if

if the channel is sufficiently short, that for a certain drain voltage

$$L \simeq y_s + y_d,$$

condition holds without occurence of avalanche breakdown in drain, the drain current is wholly governed by denomenatc term in eqn. (5.14) that anomalously large current is predicted at punch through.

This an maly results due to dominance of drift component of current at drain depletion layer edge, which has been taken to be negligible in earlier assumption through the boundary conditions. Assuming the transition from diffusion to drift occurs over one debye length, the drain current at punch through

$$I_D = \frac{qD_n W X_i \, e^{-q\phi_f/KT}}{L - y_s - y_D + L_D} \exp[q\varphi_s/KT],$$

$$= \frac{q D_n W_i \, e^{-q\phi_f/KT} \exp[q\varphi_s/KT]}{L - \sqrt{\frac{2\epsilon_{si}(V_{bi} - \varphi_s)}{qN_A}} - \sqrt{\frac{2\epsilon_{si}(V_{bi} - \varphi_s + V_{DS})}{qN_A}} + \sqrt{\frac{\epsilon_{si} KT}{q^2 N_A}}} \qquad (5.15)$$

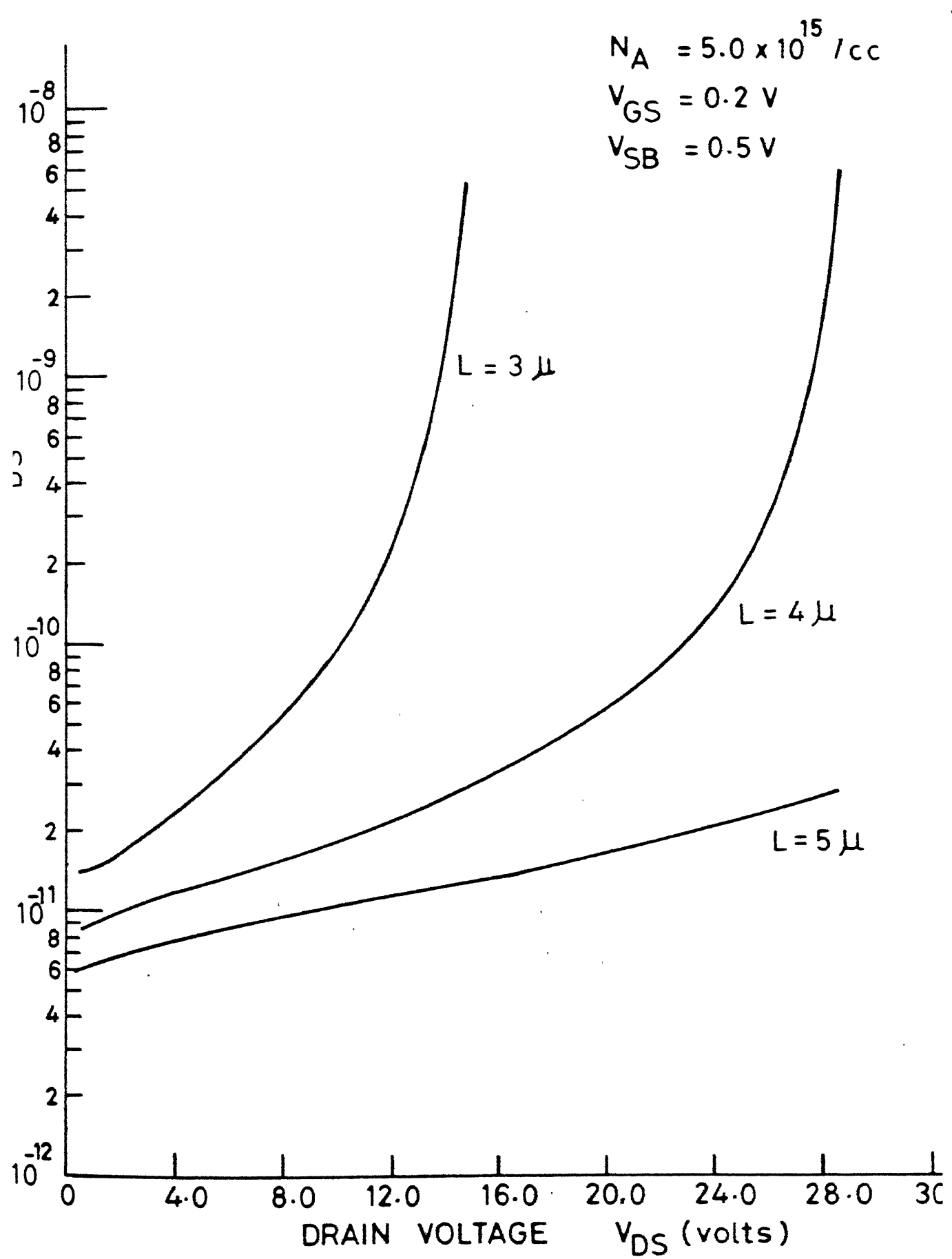


FIG. 5.1 SUBTHRESHOLD CURRENT

At the punch through, punch through voltage may be determined by using expression given in Chapter 4.

Theoretical plots of subthreshold current versus drain voltage have been shown for fixed gate voltage V_{GS}=0.2 volts. The long channel threshold voltage being 0.5 volts.

5.3 ABOVE THRESHOLD CONDUCTION

Current voltage relationship at saturation and linear region of operation has been discussed in Chapter 2. In fact the manner in which the MOSFET has developed, the observed short channel effects are not explicable from the normal gradual channel approximation. In addition to various consequences of two dimensional sharing of substrate depletion charge between the gate, source and drain regions, the charge sharing affects above threshold behaviour of MOSFET both in the linear and saturation conduction characteristics.

To clarify the situation, normalized drain current I_D^* is defined as

$$I_{DS}^* = I_{DS} \frac{L}{W} \qquad (5.16)$$

where L and W are the effective channel length and width respectively. As long as the conventional long channel

theory holds, the I^*_{DS} vs. V^*_{DS} do not depend on L and W. Thus $I_{DS} - V_{DS}$ relationship is required to be modified to include various scaled down effect.

The overall current dependence on the drain and gate voltage has been taken to be of the following nature.

i) At linear or triode region of operation

$$I_{DS} = \mu^* \frac{C_{ox}W}{L} \left[(V_{GS}-V^*_{th})V_{DS} - \frac{V^2_{DS}}{2}\right] \qquad (5.17a)$$

$$\text{for } V_{GS} - V^*_{th} \geq V_{DS} \geq 0$$

ii) At saturation

$$I_{DS} = \mu^* \frac{C_{ox}W}{2(L-\Delta L)} (V_{GS} - V^*_{th})^2 \qquad (5.17b)$$

$$\text{for } V_{DS} > V_{GS} - V^*_{th} \geq 0.$$

where μ^* effective mobility discussed in Chapter 4.

V^*_{th} = effective threshold voltage given as

$$V^*_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{2\epsilon_{si}qN_A(2\phi_f)}.K}{C_{ox}} + \Delta V_{th} \qquad (5.18)$$

The factor K consists of one or more factors corresponding to various scaled down effects such as short channel effect,

narrow width effect and substrate biasing effect, as described in Chapter 3.

ΔV_{th} includes the shift in threshold voltage, due to non-uniformly doped substrate.

Finally the term ΔL, known as channel reduction term is determined as follows.

The Channel Reduction Term:

While operating in the saturation region, the output characteristics of MOS devices shows a finite differential on-resistance, the potential at the end of inversion layer will be fixed at the value $V_{D_{sat}}$. As the drain voltage is increased further, the reverse bias across the drain junction will increase, as a result the depletion region separating end of channel and drain will increase. Effective channel length thus will become shorter, resulting in an upward tilting of the current voltage characteristics beyond saturation. As it is obvious from the discussion, this phenomena is particularly important for short channel device.

Out of the various models given for predicting the channel length modulation term [31], at present an analytical model based on velocity saturation effect has been chosen. This model is more suitable for short channel MOSFETs.

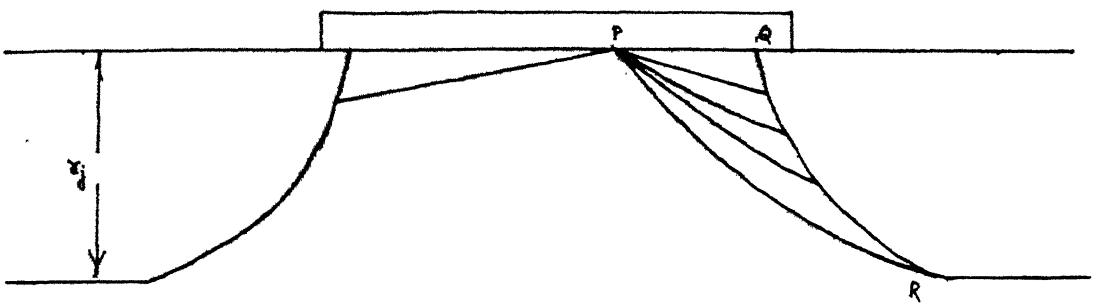


Fig. 5.2 Diagram for Channel Length Modulation

This model is based upon the assumption that carrier velocities saturate in the channel. The velocity saturation is apparently, field dependent and occurs at some critical field strength E_o.

For simplicity it has been assumed that the channel of MOSFET in saturation MODE is composed of only two regions. The normal channel, and the space charge region L, as shown in the Fig. 5.2.

In the space charge region there is a two dimensional current flow near the drain and carriers are spread in the region PQR. This bulk conduction effect may be attributed to two dimensional electric field distribution. As a consequence of this bulk conduction, it becomes necessary to include the contribution of the mobile charges to the drain substrate depletion charge. Including it in Poisson's equation

$$\frac{d^2V(y)}{dy^2} = \frac{1}{\epsilon_{si}} \left(qN_A + \frac{J(y)}{v_{sat}} \right)$$

where,

$J(y)$ = current density

v_{sat} = carrier saturation velocity

the differential equation may be written as

$$\frac{d^2V(y)}{dy^2} = \frac{1}{\epsilon_{si}} \left(qN_A + \frac{I_{D_{sat}}}{W \cdot v_{sat} \cdot r_j}\right) \qquad (5.19)$$

and may be solved using following boundary conditions

$$-\frac{dv}{dy}\Big|_{L-\Delta L} = E(y)\Big|_{L-\Delta L} = E_o$$

$$V(L) = V_{DS} + V_{bi}$$

$$V(L-\Delta L) = V_{D_{sat}}$$

Thus $V(L) - V(L-\Delta L) = (V_{DS} + V_{bi} - V_{D_{sat}})$

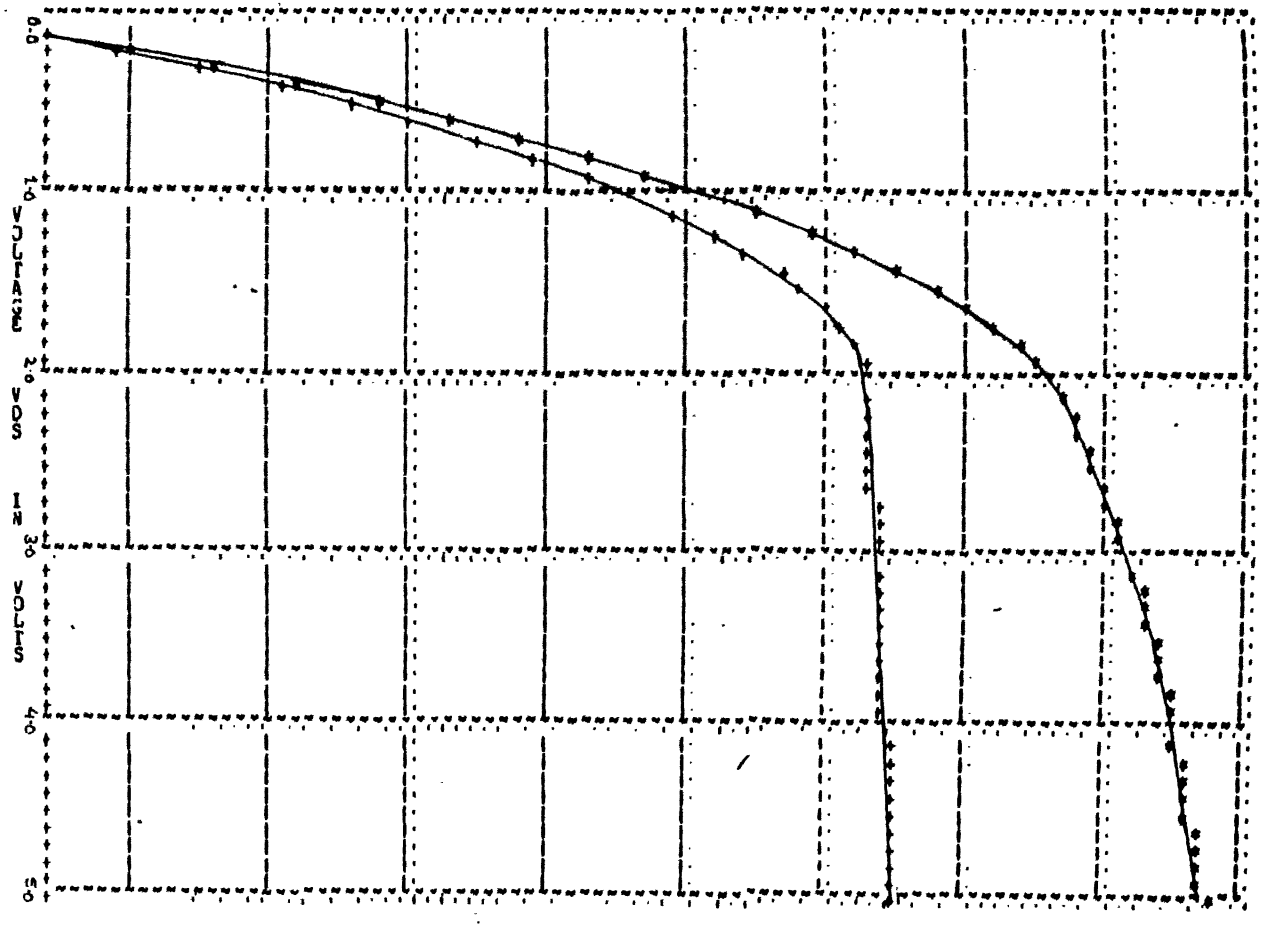
Integration of eqn. (5.19) twice with boundary conditions result in a quadratic equation in ΔL.

$$\frac{1}{\epsilon_{si}} \left(qN_A + \frac{I_{D_{sat}}}{W \cdot r_j \cdot v_{sat}}\right) (\Delta L)^2 + E_o(\Delta L) + (V_{DS} + V_{bi} - V_{D_{sat}}) = 0 \qquad (5.20)$$

L may be obtained by solving (5.20)

$$\Delta L = \frac{\left[E_o^2 + \frac{1}{\epsilon_{si}} \left(qN_A + \frac{I_{D_{sat}}}{W \cdot r_j \cdot v_{sat}}\right)(V_{DS} + V_{bi} - V_{D_{sat}})\right]^{1/2} - E_o}{\frac{1}{\epsilon_{si}} \left(qN_A + \frac{I_{D_{sat}}}{W \cdot r_j \cdot v_{sat}}\right)} \qquad (5.21)$$

ID51 I AMPS.@	ID52 I AMPS.@
0.00000E+00	0.00000E+00
5.90226E-05	5.49112E-05
1.45672E-04	1.05307E-04
1.69568E-04	1.65038E-04
2.21132E-04	2.02352E-04
2.69699E-04	2.43552E-04
3.16077E-04	2.83033E-04
3.59208E-04	3.23455E-04
4.00330E-04	3.63809E-04
4.37955E-04	4.03957E-04
4.73708E-04	4.43355E-04
5.05822E-04	4.83233E-04
5.36188E-04	5.22885E-04
5.62736E-04	5.62552E-04
5.87566E-04	6.02057E-04
6.08514E-04	6.41731E-04
6.26724E-04	6.81301E-04
6.43411E-04	7.20951E-04
6.55899E-04	7.60611E-04
6.67077E-04	8.00265E-04
6.73839E-04	8.39915E-04
6.77944E-04	8.79560E-04
6.85188E-04	9.19232E-04
6.89544E-04	9.58872E-04
6.93926E-04	9.98537E-04
6.98097E-04	1.03819E-03
7.02377E-04	1.07785E-03
7.06692E-04	1.11751E-03
7.11055E-04	1.15715E-03
7.15488E-04	1.19682E-03
7.19938E-04	1.23645E-03
7.24566E-04	1.27613E-03
7.29074E-04	1.31577E-03
7.32114E-04	1.35538E-03
7.35034E-04	1.39507E-03
7.37884E-04	1.43472E-03
7.40552E-04	1.47435E-03
7.43179E-04	1.51403E-03
7.45694E-04	1.55368E-03
7.48144E-04	1.59334E-03
7.50514E-04	1.63297E-03
7.52926E-04	1.67264E-03
7.55056E-04	1.71230E-03
7.57224E-04	1.75196E-03
7.59344E-04	1.79162E-03
7.61394E-04	1.83128E-03
7.63402E-04	1.87093E-03
7.65356E-04	1.91060E-03
7.67266E-04	1.95025E-03
7.69126E-04	1.98993E-03



THESE D.C. CHARACTERISTICS WERE CALCULATED FOR THE FIXED GATE VOLTAGE "VGS" OF 2.00000E+00 VOLTS.

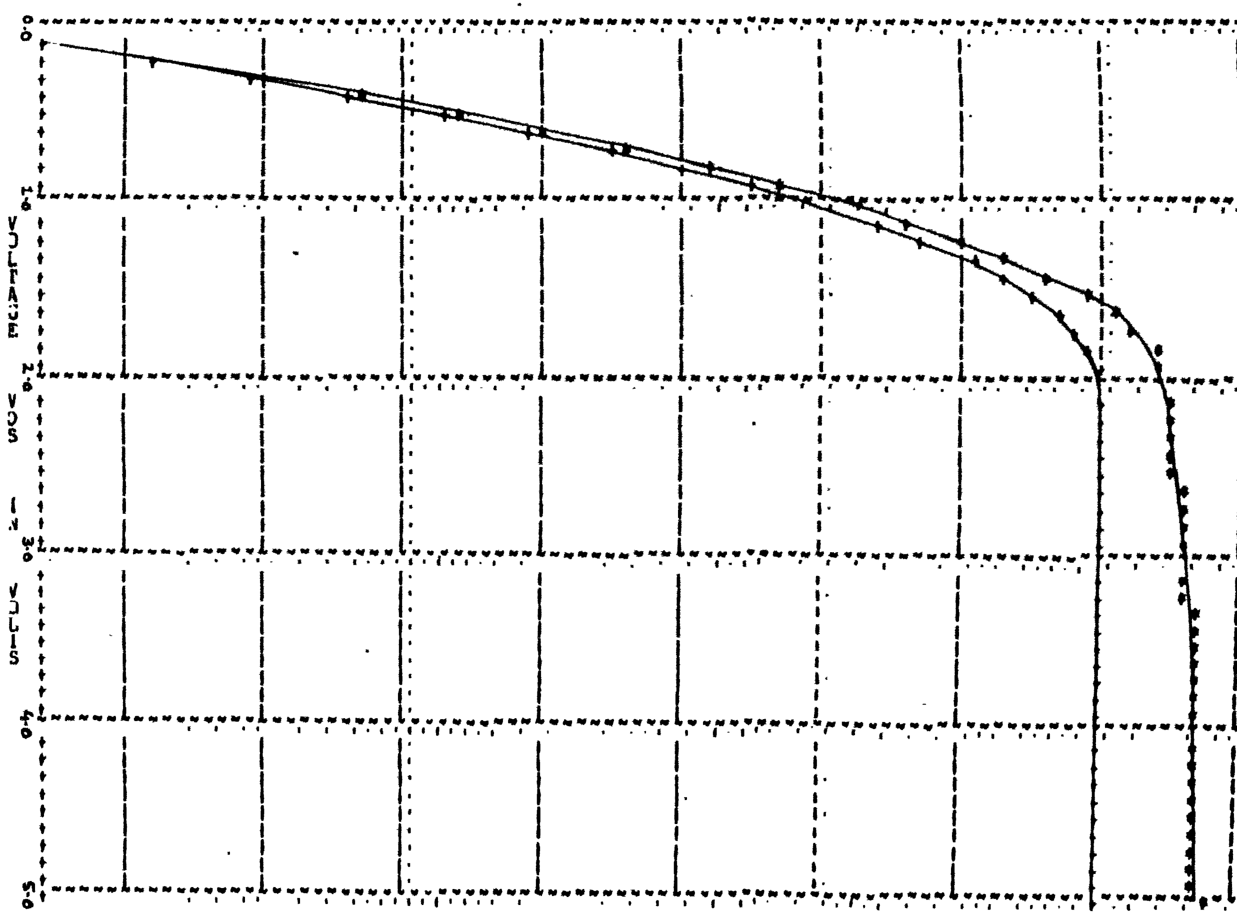
THE MAIN MOSFET PARAMETERS USED IN THIS SIMULATION ARE SPECIFIED BELOW :

THE DEVICE OPERATING TEMPERATURE IN DEGREES KELVIN IS ----------	5.00000E+02
THE GATE OXIDE THICKNESS IN CMS. IS ----------	5.00000E-06
THE SOURCE/DRAIN DIFFUSION DEPTH IN CMS. IS GIVEN AS ----------	8.00000E-05
THE APPLIED SUBSTRATE POTENTIAL IN VOLTS IS TAKEN AS ----------	-4.00000E+00
THE CRYSTAL ORIENTATION OF THE SILICON MOSFET IS ----------	<100>
THE BULK DOPING LEVEL OF THE SUBSTRATE PER CC. IS TAKEN AS ----------	1.00000E+16

ID51 .... DRAIN CUR. FOR SHORT CHANNEL MOSFET, L=2.0 MICRONS, W=8.0MICRONS.

ID52 .... DRAIN CUR. FOR LONG CHANNEL MOSFET, L=8.0 MICRONS, W=32.0 MICRONS.

IDS1 (AMPS.)	IDS2 (AMPS.)
0.0000E+00	0.0000E+00
3.4318E-05	3.0555E-05
6.6857E-05	5.5148E-05
9.7550E-05	9.8360E-05
1.2648E-05	1.2341E-05
1.5351E-05	1.4257E-05
1.7830E-05	1.7383E-05
2.0216E-05	1.9524E-05
2.2381E-05	2.1394E-05
2.4348E-05	2.3349E-05
2.6117E-05	2.5229E-05
2.7746E-05	2.6713E-05
2.9173E-05	2.8023E-05
3.0407E-05	2.9135E-05
3.1473E-05	3.0065E-05
3.2332E-05	3.0832E-05
3.3005E-05	3.1349E-05
3.3513E-05	3.1715E-05
3.3821E-05	3.1387E-05
3.3971E-05	3.1323E-05
3.4032E-05	3.1339E-05
3.4089E-05	3.1353E-05
3.4115E-05	3.1355E-05
3.4201E-05	3.1379E-05
3.4256E-05	3.1392E-05
3.4311E-05	3.2025E-05
3.4366E-05	3.2013E-05
3.4422E-05	3.2031E-05
3.4478E-05	3.2041E-05
3.4533E-05	3.2053E-05
3.4591E-05	3.2071E-05
3.4649E-05	3.2085E-05
3.4705E-05	3.2093E-05
3.4738E-05	3.2103E-05
3.4759E-05	3.2112E-05
3.4798E-05	3.2113E-05
3.4826E-05	3.2123E-05
3.4854E-05	3.2131E-05
3.4880E-05	3.2135E-05
3.4905E-05	3.2142E-05
3.4929E-05	3.2147E-05
3.4952E-05	3.2152E-05
3.4975E-05	3.2157E-05
3.4997E-05	3.2152E-05
3.5018E-05	3.2157E-05
3.5038E-05	3.2171E-05
3.5058E-05	3.2175E-05
3.5078E-05	3.2180E-05
3.5096E-05	3.2184E-05
3.5114E-05	3.2188E-05



THESE D.C. CHARACTERISTICS WERE CALCULATED FOR THE FIXED GATE VOLTAGE "VGS" OF 2.0000E+00 VOLTS.

THE MAIN MOSFET PARAMETERS USED IN THIS SIMULATION ARE SPECIFIED BELOW :

THE DEVICE OPERATING TEMPERATURE IN DEGREES KELVIN IS ------------- 300.00E+00
THE GATE OXIDE THICKNESS IN CMS. IS ------------------------- 5.0000E-06
THE SOURCE/DRAIN DIFFUSION DEPTH IN CMS. IS GIVEN AS ------------- 6.0000E-05
THE APPLIED SUBSTRATE POTENTIAL IN VOLTS IS TAKEN AS ------------- -1.0000E+00
THE CRYSTAL ORIENTATION OF THE SILICON MOSFET IS ------------- <100>
THE BULK DOPING LEVEL OF THE SUBSTRATE PER CC. IS TAKEN AS ---------- 1.0000E+15

IDS1 ..... DRAIN CUR. FOR NARROW WIDTH MOSFET, W=2.0 MICRONS L=8.0 MICRONS.

IDS2 ..... DRAIN CUR. FOR WIDE WIDTH MOSFET, W=8.0 MICRONS L=8.0 MICRONS.

Fig. 5.4

The current $I_{D_{sat}}$ from (5.17b)

$$I_{D_{sat}} = \frac{\mu^* C_{ox}}{2[L-\Delta L]} (V_{GS}-V^*_{th})^2 \qquad (5.22)$$

A simultaneous solutions of above two equations will determine the saturation current level $I_{D_{sat}}$ and channel length reduction ΔL.

$I_{DS} - V_{DS}$ characteristics have been shown in Figs. (5.3) - (5.4), based on computer calculations.

The effect of channel length reduction on current voltage characteristics has been shown in Fig. 5.3.

Fig. 5.4 shows the effect of channel width reduction on current level.

For both the cases the W/L ratio is fixed.

CHAPTER 6

INFLUENCE OF HIGHER ORDER EFFECTS ON CIRCUIT PERFORMANCE

6.1 INTRODUCTION

Continuing improvement in MOS fabrication technology have made possible steady reduction in the internal dimensions of semiconductor devices. The trend towards progressively smaller internal dimensions is likely to continue for some years until fundamental physical limitation of transistors are approached. As the device size reduces, it affects the various parameters governing the circuit performance of the device. In this chapter influence of few such parameters on circuit performance have been considered.

The basic circuit chosen for the discussion is the simple MOS inverter. It is sufficient to serve the present purpose, since the inverter is the basic circuit from which most MOS logic circuits are developed. The MOS inverter exhibits all the essential features of MOS logic gates except for logic functions. Subsequent extention of MOS inverter concepts to NOR and NAND gate is simple.

6.2 INFLUENCE OF THRESHOLD VOLTAGE

The threshold voltage behaviour for short channel MOSFET has been discussed in Chapter 3 in detail. Apart from the wide variation of threshold voltage with device down scaling, it also varies considerably with operating point of the circuit due to drain and substrate biasing effects. In this section, effect of threshold voltage variation due to device minimization effect on inverter characteristic has been given.

The load device, in an inverter is used as a current source. Its threshold voltage is tailored by ion-implantation to provide a specific saturation current level. For simplicity this device is assumed to have negligible effect on overall characteristic due to threshold voltage shift. Important parameters such as noise margin, logic threshold and logic swing are then governed by threshold voltage of driver device. A variation in threshold voltage of driver device will reflect its effect on the entire characteristic of the inverter.

As an illustrative example, two inverters have been considered with different channel geometries. The depletion load device has been taken same for both cases also the

aspect ratio (w/L) is same for both the inverters. The parameters for load device are as follows:

Channel length L =20 microns

Channel width w = 5 microns

Uniform substrate doping $N_A = 1x10^{16}/cc$

Gate oxide thickness $T_{ox} = 500\ A^o$

Threshold voltage $V_{th} = -2.5$ volts

The parameters for driver device are listed in Table 6.1.

Threshold voltages have been calculated by using models developed in Chapter 3. Transfer characteristics of both inverters are drawn analytically and plotted in Fig. 6.1.

Calculated specifications for both the inverters are listed in Table 6.2.

Apparently there is a considerable change in inverter parameters due to down scaling.

6.3 INFLUENCE OF SUBTHRESHOLD CURRENT

Due to subthreshold conduction mechanism, MOS transistor drain current does not go to zero at $V_{GS} = V_{th}$ but falls of exponentially. For long channel devices, this current is of the order of a few tens of pico amps,

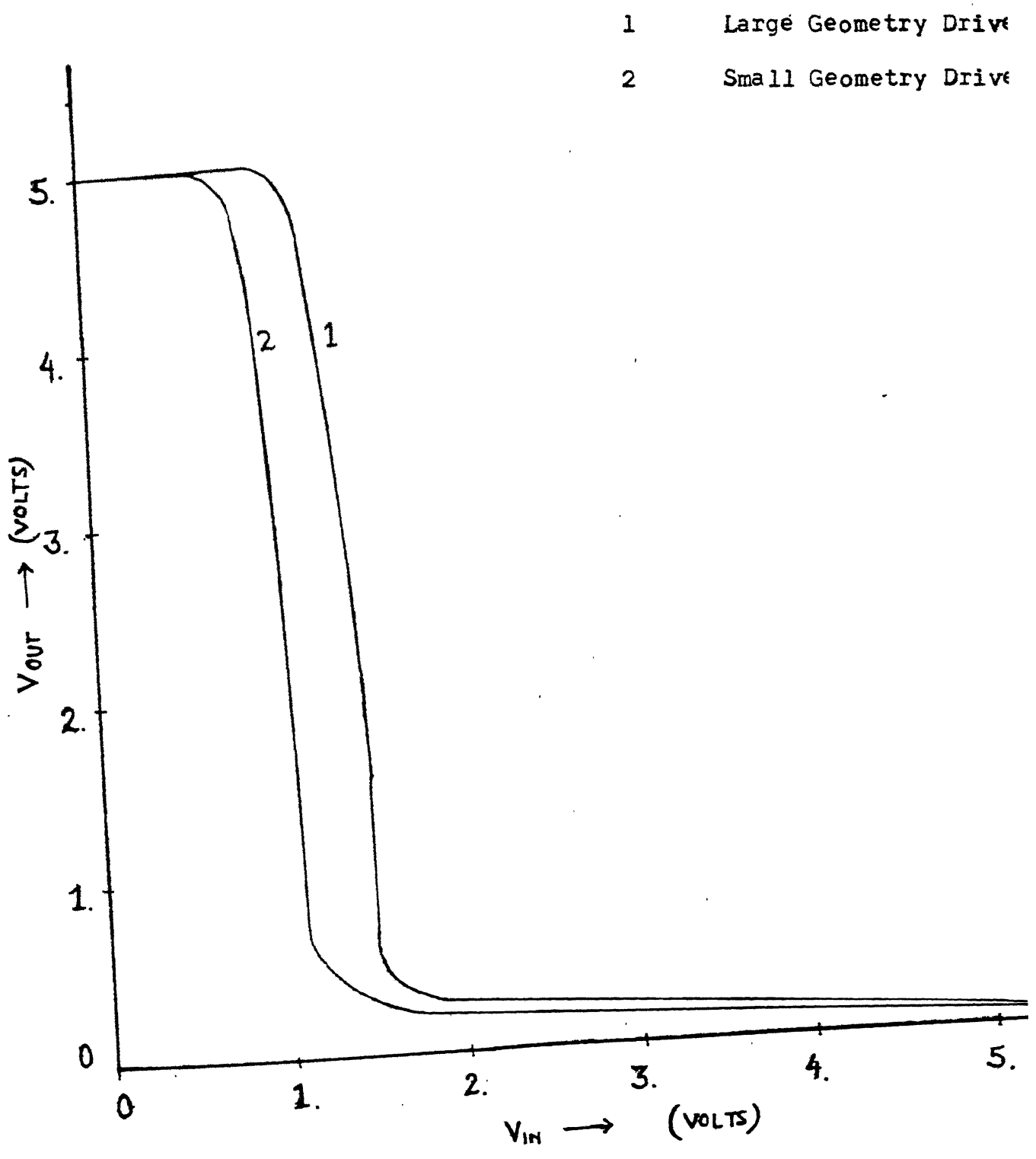


Fig. 6.1 Inverter Transfer Characteristics

Table 6.1

Basic set of specification used for the Illustrative Example

Parameter	I Large geometry device	II Small geometry device
Channel length L	8 microns	1 micron
Channel width "	64 microns	8 microns
Uniform substrate doping N_A	$1x10^{16}$/cc	$1x10^{16}$/cc
Gate oxide thickness T_{ox}	500 A^o	500 A^o
Junction depth r_j	0.5 micron	0.5 micron
Substrate bias V_{SB}	1.0V	1.0V

Table 6.2

Calculated specifications for inverters I and II

Specification	Inverter I	Inverter II
Threshold voltage of Driver device	0.96V	0.59V
Logic threshold	1.4019V	1.03194V
Noise margin NM_1	1.15V	0.6V
Noise margin NM_2	3.4V	3.8V

hence insignificant. For short channel length devices, subthreshold current rises to much higher level, even to the order of microamps. The effect of subthreshold current is more serious for dynamic circuits, where the magnitude of subthreshold conduction current results in a poor refresh times and poor long cycle operation. For a reasonably safe operation, the value of subthreshold current at $V_{GS} = 0$ is designed to be at least 10^{-5} times smaller than the current around $V_{GS} = V_{th}$.

Among the various other higher order effects, the field dependent mobility phenomena plays a vital role in circuit performance. The reduction in current levels due to this effect increases the noise margin, while the capacitive charging and discharging time becomes higher.

CHAPTER 7

CONCLUSION

A CAD model of a MOS transistor is a trade-off between simplicity and accuracy. For earlier long channel devices, the gradual channel approximation with one dimensional theory was satisfactory. However with the advancement in technology, devices have become smaller and a two dimensional analysis with other higher order effects have become necessary. In fact only a numerical solution method achieves sufficiently high accuracy but then at the cost of simplicity. On the other hand, integrated circuit designers continuously ask for simple but accurate device models in order to have aids amenable for circuit simulators.

The latter requirement has been the motivation for present work, where we have tried to focus our attention in studying and understanding various physical phenomena, originated as a result of scaling down the device size and also development of several proposed analytical and pseudo-analytical small dimension MOSFET models. To minimize the undesirable impacts of higher order effects a careful and proper selection of device parameters is required. A deep understanding of physical aspect helps to know each such

parameter and also identifies the various factors which control the MOSFET electrical behaviour. These parameters with the accurate model can be used for integrated circuit design.

The models which we have developed for the scaled down versions of the MOSFETs, therefore, assume sufficient importance. They link various electrical characteristics of such devices, directly with physical phenomena and of course a better insight into the mechanism is an added advantage. For example, the theoretical plots in Chapter 3, give a first order estimate of an important parameter, the threshold voltage for various combinations of other parameters, valid upto very small device dimensions. Similarly the models in Chapter 4, provide a guideline for safe operation of the device.

We can summerize the important points of the work into following steps:

1. For the short channel MOSFETs, the threshold voltage decreases as channel length decreases. For such devices, threshold voltage decreases as substrate doping concentration, gate oxide thickness and substrate bias voltage but increases with decreasing drain voltage and junction depth.

2. For the narrow width MOSFETs, the threshold voltage increases as channel width decreases. This influence is higher at increased substrate doping concentrations. Hence the threshold voltage sensitivity to the substrate bias is increased for such devices.

3. For small geometry MOSFETs punch through occurs more easily as the substrate doping concentration and channel length decreases. The required drain voltage values for the punch through are larger than the required substrate bias.

4. The source drain breakdown voltage of the short channel MOSFET is greatly reduced by decreasing the channel length L. To improve the breakdown voltage the resistance of the substrate R_{sub} can be minimized, so that potential drop across R_{sub} due to substrate current remains smaller than 0.6V. The use of shallower source and drain reduces the probability of corner breakdown phenomenon.

5. To reduce oxide charging due to hot carrier effects, the density of water related traps in the oxide should be minimized, because such traps are known to capture electrons. Design of a circuit consistent with the hot electron limitation is for same circuits, nontrivial. The 1 μm technology may be expected to run with a drain

supply voltage V_{DD} of about 2.5V. For conventional circuits this voltage sets the upper bound on both V_{GS} and V_{DS}. Thus circuits are unconditionally safe as hot electrons are concerned. Also extremely shallow source/drain junction is found to increase hot carrier junction phenomenon.

6. For short channel devices the subthreshold current depends on drain voltage for $V_{DS} > 3KT/q$, unlike the long channel devices. This may be attributed to early punch through in such devices. An appropriate increase in doping level thus, helps checking large subthreshold current to an extent. The subthreshold characteristics are important for utilizing devices in logic circuitry. However simple linear scaling of a device is insufficient to hold subthreshold current to an acceptable level. Many factors such as band gap, temperature, interface charge and diffusion profiles are not scalable parameters but they have a profound influence on device performance in subthreshold region.

Finally, we conclude with a mention of the scope of future work on this topic. The aspects which we have covered

here, appropriate numerical models can be developed for them, based upon the study already made. Such models will give more accurate results at a cost of increased computation time. A closed form relationship for hot electron effect may also be useful. Another useful and interesting area to work on will be development of computer programs for the transient/ small signal analysis and automated parameter selection of scaled down MOSFETs.

APPENDIX A

Short Channel MOSFET Calculations:

The relevant diagram is shown in Fig. 1. The charge sharing factor F is given by

$$F = \frac{\text{Area}(AB'C'D)}{\text{Area}(ABCD)}$$

$$= \frac{L_{eff} + L'}{2L_{eff}} \qquad (1)$$

From simple geometry

We get for small drain voltage ($L_1 = L_2$)

$$L_1 = [(r_j+W_s)^2 - X_{dm}]^{1/2} - r_j - X_s$$

$$L' = L_{eff} - 2L$$

hence,

$$F = \frac{[(r_j+W_s)^2 - X_{dm}^2]^{1/2} - r_j - X_s}{L-2X_s} \qquad (2)$$

For a larger drain voltage $L_2 > L_1$

the charge sharing factor

$$F = 1 - \frac{L_1+L_2}{2L_{eff}} \qquad (3)$$

APPENDIX A

Short Channel MOSFET Calculations:

The relevant diagram is shown in Fig. 1. The charge sharing factor F is given by

$$F = \frac{\text{Area}(AB'C'D)}{\text{Area}(ABCD)}$$

$$= \frac{L_{eff} + L'}{2L_{eff}} \qquad (1)$$

From simple geometry

We get for small drain voltage ($L_1 = L_2$)

$$L_1 = [(r_j+W_s)^2 - X_{dm}]^{1/2} - r_j - X_s$$

$$L' = L_{eff} - 2L$$

hence,

$$F = \frac{[(r_j+W_s)^2 - X_{dm}^2]^{1/2} - r_j - X_s}{L-2X_s} \qquad (2)$$

For a larger drain voltage $L_2 > L_1$

the charge sharing factor

$$F = 1 - \frac{L_1+L_2}{2L_{eff}} \qquad (3)$$

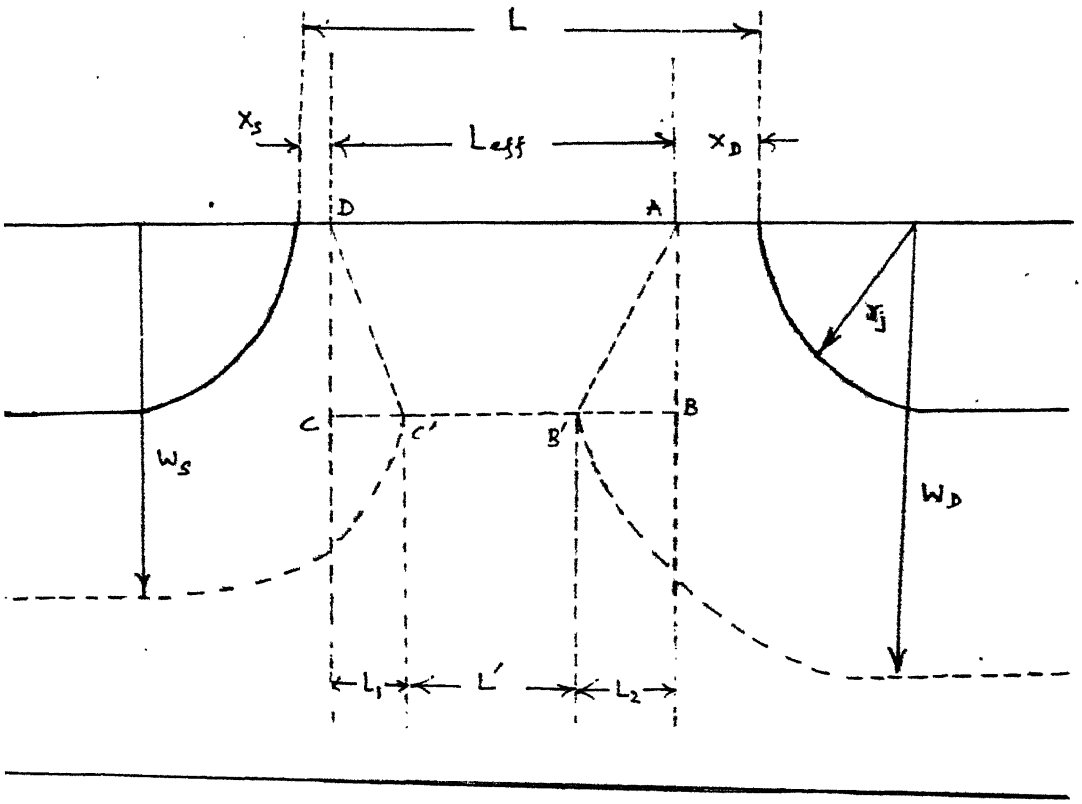


Fig 1 : Short Channel Schematic

Again from geometrical considerations

$$(X_s+r_j+L_1)^2 + X_{dm}^2 = (r_j+W_s)^2 \tag{4a}$$

$$(X_d+r_j+L_2)^2 + X_{dm}^2 = (r_j+W_D)^2 \tag{4b}$$

Solving equation (4)

$$L_1 = [(r_j+W_s)^2 - X_{dm}^2]^{1/2} - r_j-X_s \tag{5a}$$

$$L_2 = [(r_j+W_D)^2 - X_{dm}^2]^{1/2} - r_j-X_D \tag{5b}$$

The charge sharing factor F becomes

$$F = 1 - \frac{[(r_j+W_s)^2- X_{dm}^2]^{1/2}+[(r_j+W_D)^2-X_{dm}^2]^{1/2}-2r_j-X_s-X_D}{2(L-X_s-X_D)} \tag{6}$$

If the backgate bias is high enough the surface of the depletion region under the gate electrode become triangular. The depth of the depletion region at the onset of this transition (i.e. L'=0) can be determined by

$$L_1 + L_2 = L_{eff} \tag{7}$$

Substituting equation (5) in (7) and solving for X_{dm}

$$W_{dm} = \frac{\left\{[2(2r_j+W_s+W_D)^2]^2-[(L+2r_j)^2-(r_j+W_s)-(r_j+W_D)^2]^2\right\}^{1/2}}{2(L+2r_j)} \qquad (8)$$

Derivation of W_s and W_D:

In cylindrical coordinates Poisson's equation is written as

$$\frac{1}{r}\frac{\partial(\frac{\partial rV(r)}{\partial r}}{\partial r} = \frac{qN_A}{\epsilon_{si}}$$

$$\text{i.e.} \quad \frac{\partial V(r)}{\partial r} = \frac{qN_A r^2}{2\epsilon_{si}} + C_1$$

With boundary condition at the source end

$$\left.\frac{\partial V(r)}{\partial r}\right|_{r=r_j+W_s} = E(r_j+W_s) = 0$$

$$\frac{\partial V(r)}{\partial r} = \frac{qN_A r}{2\epsilon_{si}} - \frac{qN_A}{2\epsilon_{si}}\frac{(r_j+W_s)^2}{r} \qquad (9)$$

Integrating (9) between limits r_j to r_j+W_s

$$2\epsilon_{si}\frac{(V_{bi}+V_{SB})}{qN_A} = \frac{r_j^2-(r_j+W_s)^2}{2} + (r_j+W_s)^2 \ln\left(\frac{r_j+W_s}{r_j}\right) \qquad (10)$$

Similarly for drain side

$$\frac{2\epsilon_{si}(V_{bi}+V_{SB}+V_{DS})}{q N_A} = \frac{r_j-(r_j+W_D)^2}{2} + (r_j+W_D)^2 \ln\left(\frac{r_j+W_D}{r_j}\right) \tag{11}$$

Source and drain depletion layer width W_s and W_D may be evaluated from equations (10) and (11) by any suitable iteration method.

Narrow Width Calculations:

The schematic diagram is shown in Fig. 2. The tapered oxide region extends over a distance of (b-a) units in the horizontal direction while the $Si-SiO_2$ place has been taken at a height of Y_{res}.

The charge Q_{TAP}, contained in the triangle is expressed by following integral.

$$Q_{TAP} = q \int_0^L \int_a^b \int_{y_1}^{y_2} N_A dx\, dy\, dz$$

$$= \frac{q N_A X_{dm} L (b-a)}{2} \text{ couls} \tag{12}$$

Charge under thin oxide is as usual

$$Q_B = q N_A X_{dm} W.L \quad \text{couls.} \tag{13}$$

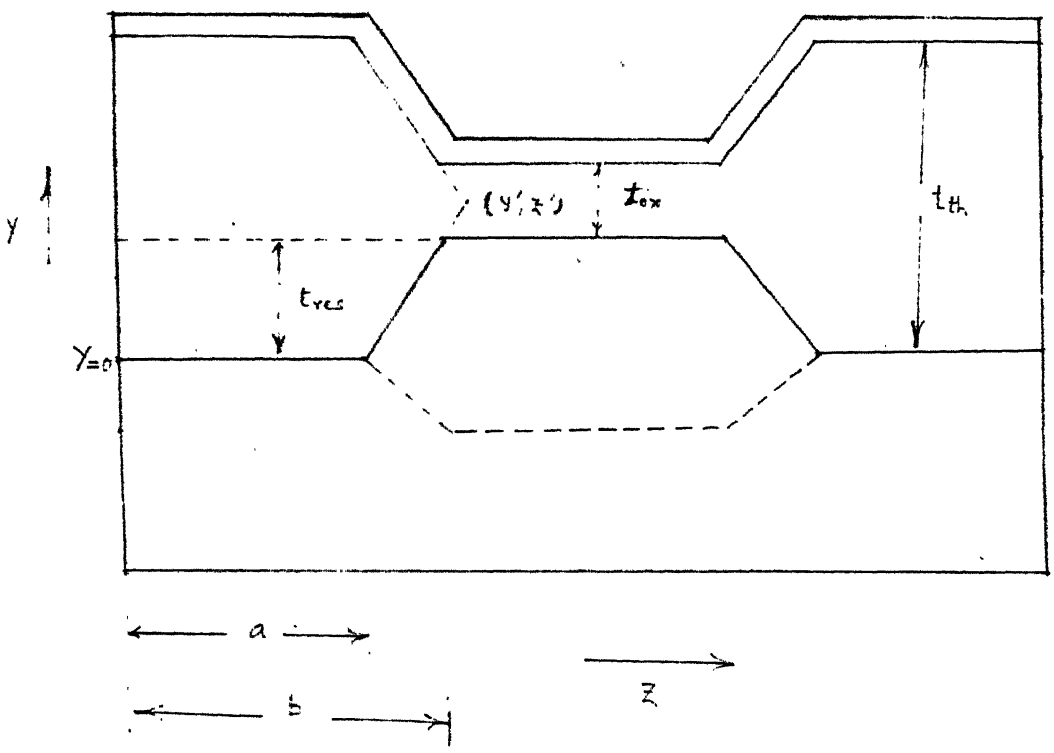


Fig 2 : Narrow Width Schematic

C_{TAP} may be calculated by considering capacitor model shown in Fig. 3. The capacitor C_{TAP} is a series combination of infinitesimal small capacitances as shown in Fig. These capacitances are further devided into infinitesimal small parallel capacitances.

One such combination of parallel capacitance may be written as

$$dc = \int_{x=R-t}^{R} \frac{\epsilon_{ox} \cdot L \cdot dx}{x \cdot d\delta} \tag{14}$$

The total capacitance is thus

$$\frac{1}{C_{TAP}} = \Sigma \frac{1}{dc} \tag{15}$$

Evaluating R, t, and δ geometrically

$$C_{TAP} = \epsilon_{ox} \frac{L d'}{\delta} \ln \left[\frac{2d'b+f}{2d'a+f} \right] \tag{16}$$

Where $d' = 1+d^2$ (17a)

$$d = \frac{t_{ox}+t_{res}-t_{th}}{(b-a)} \tag{17b}$$

$$f = 2dy' + 2dg - 2z' \tag{17c}$$

$$g = \frac{(t_{ox}+t_{res}).a-t_{th}.b}{(b-a)} \tag{17d}$$

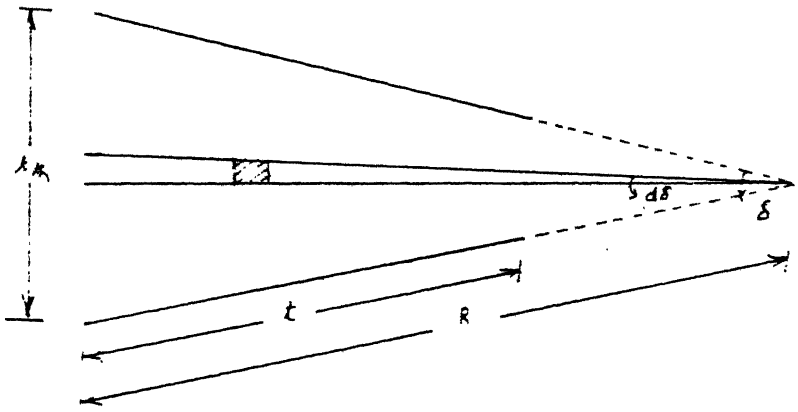


Fig 3 : Model for Tapered Oxide Capacitance Calculations.

where coordinates y' and z' are given by

$$y' = \frac{t_{res} \cdot t_{th}}{t_{th} - t_{ox}}$$

$$z' = \frac{t_{ox} \cdot a - t_{th} \cdot b}{t_{ox} - t_{th}}$$

δ , the angle between capacitor plates is

$$\delta = - \tan^{-1} \left(\frac{t_{res}}{b-a}\right) - \tan^{-1} \left(\frac{t_{th}-y}{z-a}\right) \qquad (17e)$$

Derivation of Surface Potential:

From eq. (3.23)

$$\frac{qN_{inv}}{C_{ox}} = V_{G_I} - \varphi_{S_I} - \frac{a}{V_T} \left(\frac{\varphi_{SI}}{V_T} - m_1 - 1\right)^{1/2} + \frac{m_o}{\sqrt{2}} \qquad (18)$$

and

$$\frac{qN_{inv}}{C_{ox}} - V_{G_U} - \varphi_{S_U} \frac{a}{V_T} \left(\frac{\varphi_{S_U}}{V_T} - 1\right) \qquad (19)$$

Eliminating V_{G_I} from (18) and (3.19)

$$\frac{qN_{inv}}{V_T \cdot C_{ox}} = a \left[\left(\frac{n_i}{N_A}\right)^2 \exp\left(- \frac{V_{SB}}{V_T}\right) \exp\left(\frac{\varphi_{S_I}}{V_T}\right)\right.$$

$$+ \left[\left(\frac{\varphi_{S_I}}{V_T} - m_1 - 1 \right)^{1/2} + m_o/\sqrt{2} \right]^2 \Big]^{1/2}$$

$$- a \left[\left(\frac{\varphi_{S_I}}{KT} - m_1 - 1 \right)^{1/2} + m_o/\sqrt{2} \right] \qquad (20)$$

Similarly eliminating V_{G_U} from (19) and (3.20)

$$\frac{qN_{inv}}{C_{ox} \cdot V_T} = a \left\{ \left(\frac{n_i}{N_A} \right)^2 \exp\left(- \frac{V_{SB}}{V_T} \right) \exp\left(\frac{\varphi_{S_U}}{V_T} \right) + \left(\frac{\varphi_{S_U}}{V_T} - 1 \right)^{1/2} \right\}^{1/2}$$

$$+ \left(\frac{\varphi_{S_U}}{V_T} - 1 \right)^{1/2} - a \left(\frac{\varphi_{S_U}}{V_T} - 1 \right)^{1/2} \qquad (21)$$

Taking last term in (20) to left, squaring and taking log an iteration scheme for finding φ_{S_I} results for (I+1)th iteration.

$$\frac{\varphi_{S_I}^{I+1}}{V_T} = \frac{V_{SB}}{V_T} + 2 \ln\left(\frac{N_A}{n_i} \right) + \ln \left\{ \left[\frac{qN_{inv}}{V_T a C_{ox}} \right]^2 + 2 \left[\frac{qN_{inv}}{V_T a C_{ox}} \right] \left[\left(\frac{\varphi_{S_I}^{I}}{V_T} - m_1 - 1 \right)^{1/2} + \frac{m_o}{\sqrt{2}} \right] \right\} \qquad (22)$$

Similarly,

$$\frac{\varphi_{S_U}^{I+1}}{V_T} = \frac{V_{SB}}{V_T} + 2 \ln\left(\frac{N_A}{n_i} \right) + \ln \left\{ \left[\frac{q N_{inv}}{V_T a C_{ox}} \right]^2 + 2 \left[\frac{q N_{inv}}{V_T a C_{ox}} \right] \left(\frac{\varphi_{S_U}^{i}}{V_T} - 1 \right)^{1/2} \right\} \qquad (23)$$

A few iterations using (22) and (23) gives φ_{S_I} and φ_{S_U} results with high accuracy.

APPENDIX B

Calculation of Channel Thickness for Subthreshold Conduction:

To find the channel thickness X_i, it is necessary to consider the total charge available for conduction in the surface depletion region. By integration in the X direction over the surface depletion region the total charge Q_n is obtained as

$$Q_n = q \int_o^{X_{dm}} n_s \, e^{q(\varphi(x) - \varphi_s)/KT} \, dx$$

$$= q \sqrt{\frac{\epsilon_{si} KT}{2q^2 N_A \left(\frac{q\varphi_s}{KT} + 1\right)}} \cdot n_s \qquad (1)$$

The free charge available for conduction is thus confined to a distance from the surface of

$$X_i = \sqrt{\frac{\epsilon_{si} KT}{2q^2 N_A \left(\frac{q\varphi_s}{KT} + 1\right)}} \qquad (2)$$

which is the channel thickness.

REFERENCES

1. R.H. Dennard, F.H. Gaensslen, H. Yu, Y.L. Rideout, E. Bassons and A.R. Leblanc, 'Design of Ion-Implanted MOSFETs with very Small Dimensions', IEEE J. Solid-State Circuits, vol. SC-9, pp. 256-268, Oct. 1974.

2. G.L. Varnel, P.L. Shah and R.H. Haveman, 'MOS and Bipolar VLSI Technologies using Electron Beam Lithography', Proc. of the IEEE, vol. 17, pp. 612-639, May,1983.

3. C.A.T. Salama, 'A New Short Channel MOSFET Structure', Solid State Electronics, vol. 20, pp. 1003-1010, Dec. 1977.

4. K.Y. Chiu, K.L. Moll and J. Monoliu, 'A Birds Beak Free Local Oxidation Technology Feasible for VLSI Circuits', IEEE Trans. Elect. Devices, vol. ED-29, pp. 536-540, April,1982.

5. D.H. Hodges and H.G. Jackson, 'Analysis and Design of Digital Integrated Circuits', McGraw Hill, 1983.

6. 'VLSI Technology', Edited by S.M. Sze, McGraw Hill, 1984.

7. L.D. Yau, 'A Simple Theory to Predict Threshold Voltage of Short Channel IGFETs. Solid State Electronics, vol. 17, pp. 1059-1063, Oct. 1974.

8. H. Lee, 'An Analysis of the Threshold Voltage for Short Channel IGFETs. Solid State Electronics, vol. 16, pp. 1407-1417, Dec. 1973.

9. G. Merckel, 'A Simple Model of the Short and Narrow Channel MOSFETs', Solid State Electronics., vol. 23, pp. 1207-1214, Dec. 1980.

10. P.P. Wang, 'Device Characteristics of Short Channel and Narrow Width MOSFET's. IEEE Trans. on Electron Devices vol. ED-25, No. 7, pp. 779-786, July,1978.

11. S.M. Sze, 'Physics of Semiconductor Devices', 2nd Edition, John Wiley and Sons Inc., 1981.

12. R.R. Troutman, 'Ion-Implanted Threshold Tailoring of IGFETs, IEEE Trans. Electron Devices., vol. ED-24, pp. 182-189.

13. H. Feltl, 'Onset of Heavy Inversion in MOS Devices Doped Non-uniformly Near the Surface', IEEE Trans. Elec. Devices, vol. ED-24, pp. 288-289, March,1977.

14. E.H. Nicollian and J.R. Brews, 'MOS (Metal Oxide Semiconductor) Physics and Technology', John Wiley and Sons Inc. , 1982.

15. T. Toyabe et.al., 'A Numerical Model of Avalanche Breakdown in MOSFETs', IEEE Trans. on Electron Devices, vol. ED-25, pp. 825-832, July,1978.

16. T. Toyabe and Shogiro Asai, 'Analytical Model of Threshold Voltage and Breakdown voltage of Short Channel MOSFETs Derived from Two-dimensional Analysis', IEEE Trans. on Electron Devices, ED-26, pp. 453-461, April,1979.

17. S.K. Ghandhi, 'Power Semiconductor Devices', John Wiley and Sons Inc., 1977.

18. S. Tam, F.C. Hsu, C. Hu, 'Hot Electron Current in very Short Channel MOSFETs', IEEE Electron Devices Letters, vol. EDL-4, pp. 249-251, July,1983.

19. Tak H. Ning, ' 1 μm MOSFET VLSI technology: Part IV Hot Electron Considerations', IEEE Trans. on Electron Devices, ED-26, pp. 346-353, April,1979.

20. E. Conwell and V.F. Weisskopf, 'Theory of Impurity Scattering in Semiconductors', Phys. Rev., vol. 77, p. 388, 1950.

21. H. Ehrenreich, 'Band Structure and Electron Transport in GaAs', Phys. Rev., vol. 120, p. 1951, 1960.

22. R.W. Coen and R.S. Muller, 'Velocity of Surface Carriers in Inversion Layers on Silicon', Solid State Electronics, vol. 23, p. 35.

23. J.R. Brews, 'Subthreshold Behaviour of Uniformly and Non-uniformly Doped Long Channel MOSFETS', IEEE Trans. on Electron Devices, ED-26, pp. 1282-1291, 1979.

24. D.A. Antoniadis and R.W. Dutton, 'SUPREM II - Models for Computer Simulation of Complete IC Fabrication Process', IEEE Trans. on Electron-Devices, vol. ED-26, pp. 490-500, April,1979.

25. J.J. Barnes, Katsushiro Shimohigashi and R.W. Dutton, 'Short Channel MOSFET in Punch-Thurough Current Mode', IEEE Trans. on Electron Devices, vol. ED-26, pp.. 446-453, April,1979.

26. R.R. Troutman and S.N. Chakravarti, 'Subthreshold Characteristics of Insulated Gate Field Effect Transistors', IEEE Trans. on Circuit Theory, vol. CT-20, pp. 659-665, Nov. 1973.

27. R.J. Van Overstrateten, G. Declerk, and C.L. Broux, 'Inadequacy of the Classical Theory of the MOS transistor Operating in weak Inversion', IEEE Trans. on Electron Devices, vol. ED-20, pp. 1150-1153, December,1973.

28. R.R. Troutman, 'Subthreshold Design Considerations for IGFETs', IEEE J. Solid State Circuits, vol. SC-9, p. 55, April,1974.

29. P. Antognetti, D.D. Caviglia and E. Profumo, 'Cad Model for Threshold Conduction in MOSFETs', IEEE J. Solid State Circuits, vol., SC-17, No. 3, June,1982.

30. D.R. Poole and D.L. KWong, 'Analytical Modelling of the Subthreshold Current in Short Channel MOSFETs', IEEE Electron Device Letters, vol. EDL-7, No. 6, June,1986.

31. L.M. Dang, 'A Simple Current Model for Short Channel IGFET and its application to circuit simulation', IEEE Trans. on Electron Devices, vol. ED-26, No. 4, pp. 436-445, April,1979.

32. Eiji Takeda, H. Kume, T. Toyabe and S. Asai, 'Submicrometer MOSFET Structure for Minimizing Hot Carrier Generation' IEEE Trans. on Electron devices, vol. ED-29, pp. 611-617, April,1982.

EE-1987-M-DAT-MOD